ECE 2300 Digital Logic and Computer Organization Fall 2024

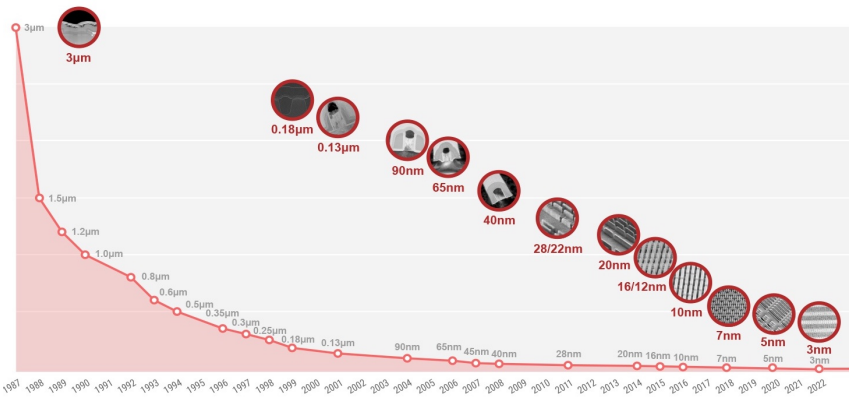
Topic 1: Digital Circuits

School of Electrical and Computer Engineering
Cornell University

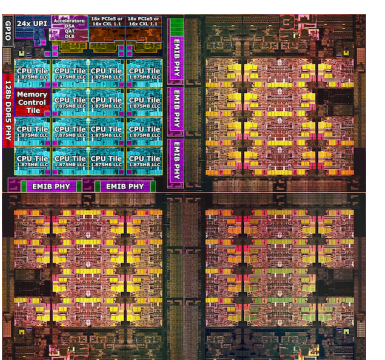
revision: 2024-08-29-04-05

1. Analog View of a Transistor

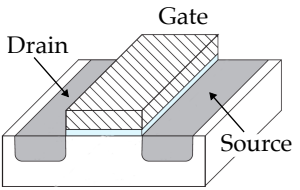
- **Transistors:** Invented by John Bardeen, Walter Brattain, and William Shockley at Bell Labs in 1947
- **Integrated Circuits:** Independently developed by Jack Kilby (at TI) and Robert Noyce (at Fairchild) in the 1950s; Noyce and Gordon Moore founded Intel in 1968

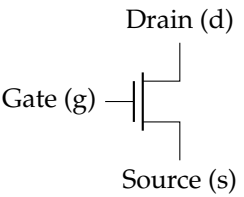


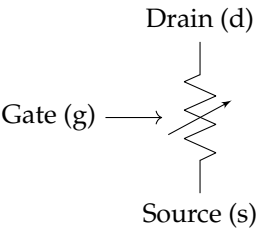
- **Intel Saphire Rapids (2023)**
  - Number of transistors: 61 billion
  - Technology node: Intel 7



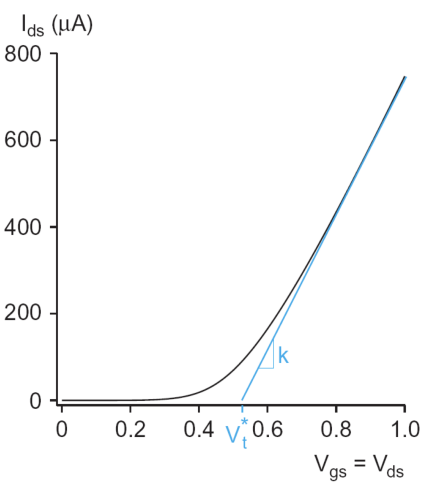
Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)





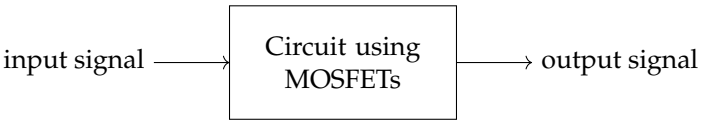


- MOS: Need three materials to make a transistor
  - _____ strong conductor of current
  - _____ insulator (does not conduct)
  - _____ conduction can be controlled
- FET: Electric field causes conduction between source and drain



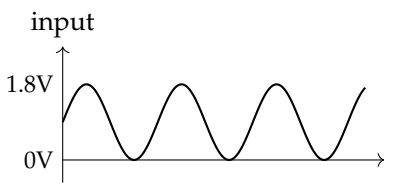
- MOSFET operation
  - As gate voltage increases, current from drain to source also increases
  - At specific threshold voltage, current starts to increase very rapidly
- MOSFET analog applications
  - Various amplifiers
  - Operational amplifiers
  - Current sources and mirrors
  - Voltage-controlled oscillators
  - Voltage regulators
  - Filters

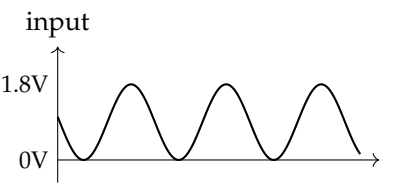
2. Digital View of a Transistor



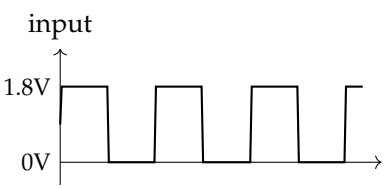
2.1. Binary Digital Abstraction

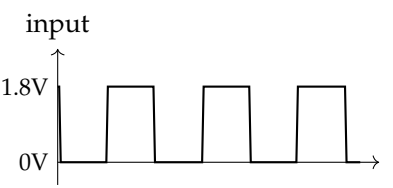
Analog circuits (continuous values are possible)



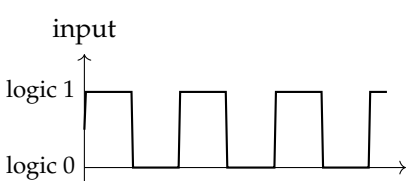


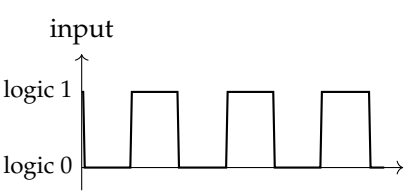
Binary digital circuits (only two specific values are possible)





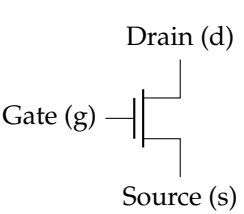
Abstract low voltage as “logic 0” and high voltage as “logic 1”

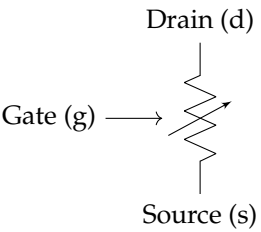


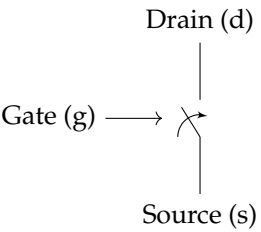


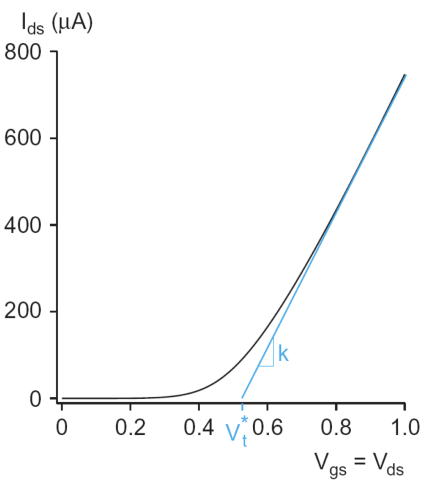
2.2. Switch-Level Model for a Transistor

- Non-linear change in current make transistors act like switches
  - If g = 0, then the switch is open
  - If g = 1, then the switch is closed

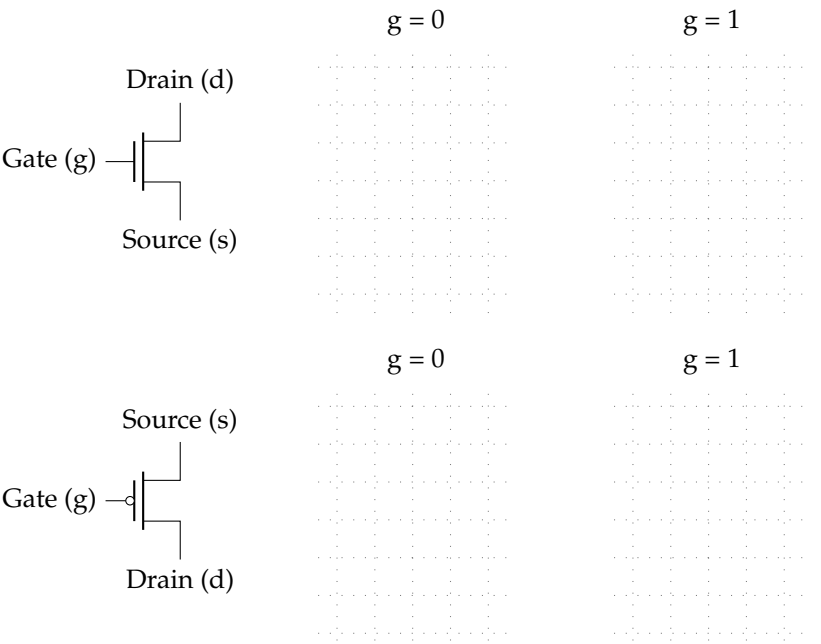








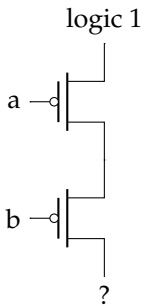
- Two different kinds of MOSFETs
  - **NMOS:** Closed when g = 1, open when g = 0, better at passing 0
  - **PMOS:** Closed when g = 0, open when g = 1, better at passing 1

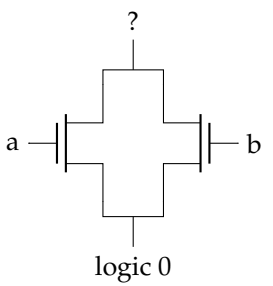


- NMOS and PMOS have complementary properties
  - For same input, one will be on and one will be off
  - Digital CMOS circuits combine NMOS and PMOS transistors

2.3. Transistor Networks

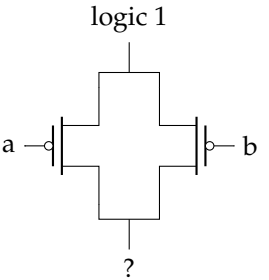
a = 0 b = 0 a = 0 b = 1 a = 1 b = 0 a = 1 b = 1





a = 0 b = 0 a = 0 b = 1

a = 1 b = 0 a = 1 b = 1

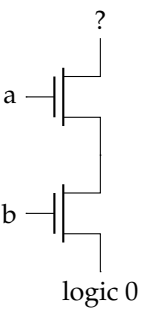


a = 0 b = 0

a = 0 b = 1

a = 1 b = 0

a = 1 b = 1



a = 0 b = 0

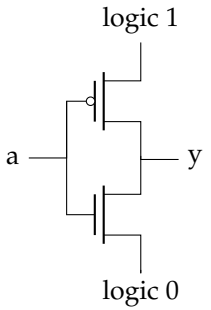
a = 0 b = 1

a = 1 b = 0

a = 1 b = 1

3. CMOS Inverter

Switch-Level Model



a = 0

a = 1

Truth Table

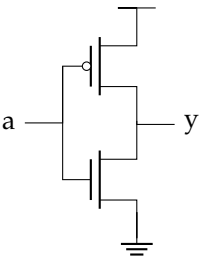
- Rows for all possible input values
- Specifies output for to given input values

a	y

Waveform

- Illustrates how outputs change over time for given input signals
- Various delay models are possible

Switch-Level Modeling in Verilog



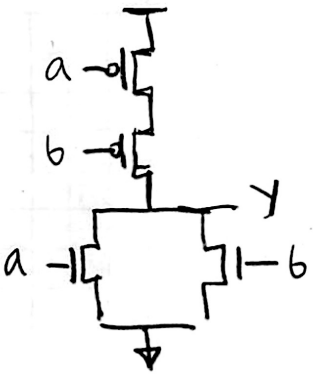

```
1  module Inverter
2  (
3    output y,
4    input  a
5  );
6
7    supply1 vdd;
8    supply0 gnd;
9
10   pmos p0( y, vdd, a );
11   nmos n0( y, gnd, a );
12
13 endmodule
```

- `supply1` is used to create a "logic 1" power supply
- `supply0` is used to create a "logic 0" ground
- `pmos( drain, source, gate )` instantiates a PMOS transistor
- `nnmos( drain, source, gate )` instantiates a PMOS transistor
- `module/endmodule` used to define a hardware module along with the corresponding input and output ports

`https://www.edaplayground.com/x/LbpL`

4. Simple Digital CMOS Circuits

Transistor-Level Schematic

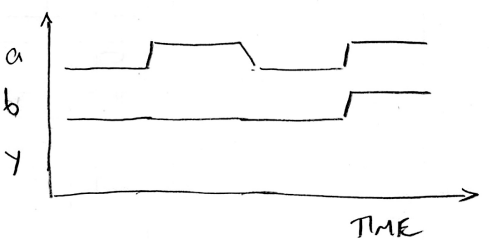


Switch-Level Model

Truth Table

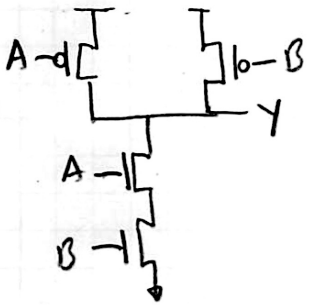
a	b	y

Waveform



https://www.edaplayground.com/x/wHkB

Transistor-Level Schematic

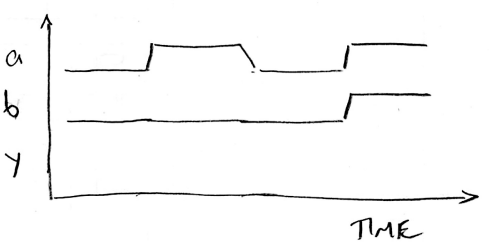


Switch-Level Model

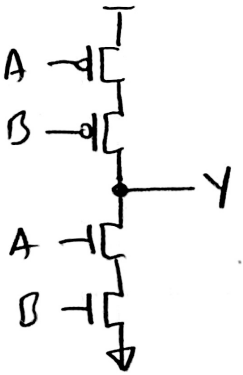
Truth Table

a	b	y

Waveform



Transistor-Level Schematic

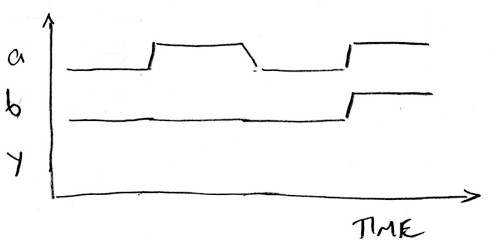


Switch-Level Model

Truth Table

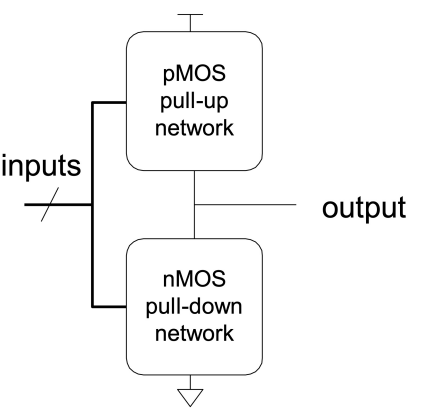
a	b	y

Waveform



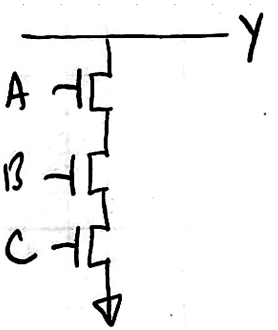
4.1. Rules for Digital CMOS Circuits

- Use NMOS and PMOS transistors such that:
  - There should never be a direct path from Vdd to ground
  - The output should never be floating
- Circuit is divided into two parts:
  - Pull-up network exclusively uses PMOS transistors
  - Pull-down network exclusively uses NMOS transistors
- The pull-up and pull-down networks are duals of each other
  - Two transistors in series in the pull-down network will be in parallel in the pull-up network
  - Two transistors in parallel in the pull-down network will be in series in the pull-up network
  - Apply these rules hierarchically to subnets
- There should always be an equal number of PMOS and NMOS transistors



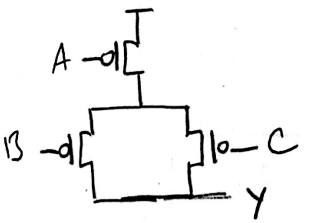
5. More Complex Digital CMOS Circuits

5.1. Multi-Input Digital Circuits



a	b	c	y

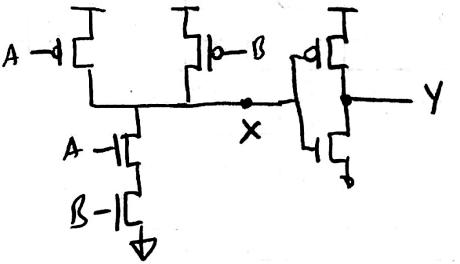
Finish the circuit using the rules for digital CMOS circuits, then fill in the truth table.



a	b	c	y

5.2. Multi-Stage Digital Circuits

Transistor-Level Schematic

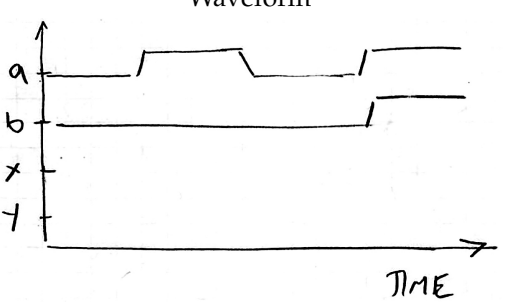


Switch-Level Model

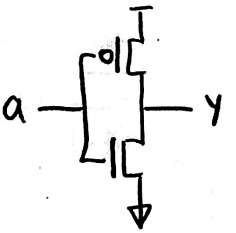
Truth Table

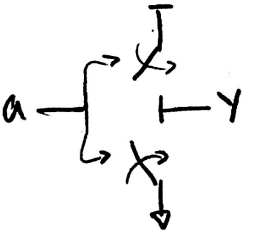
a	b	x	y

Waveform



6. Summary of Abstractions





a	Y
0	1
1	0