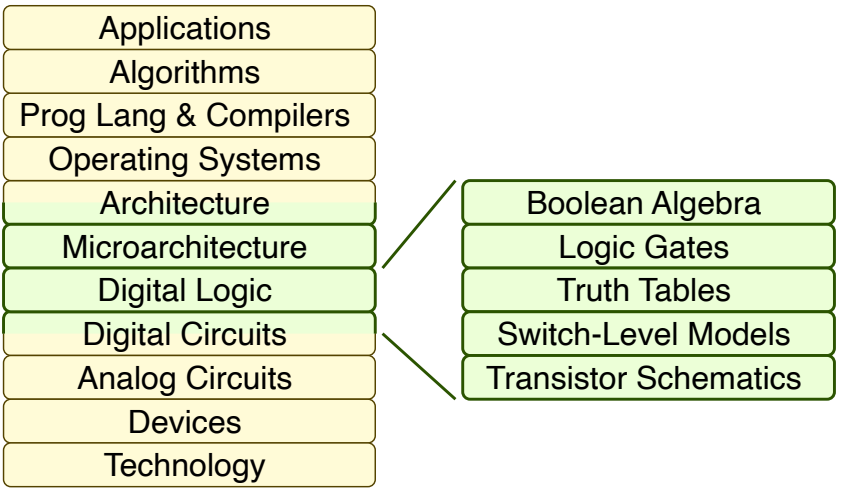
ECE 2300 Digital Logic and Computer Organization Fall 2024

Topic 1: Digital Circuits

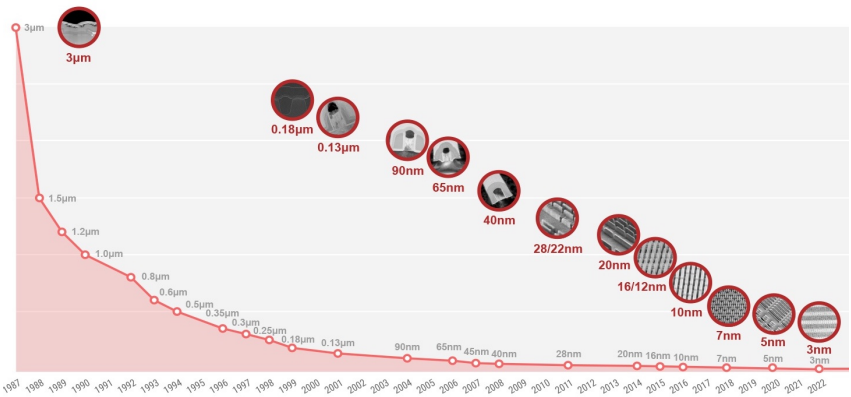
School of Electrical and Computer Engineering
Cornell University

revision: 2024-09-03-00-33

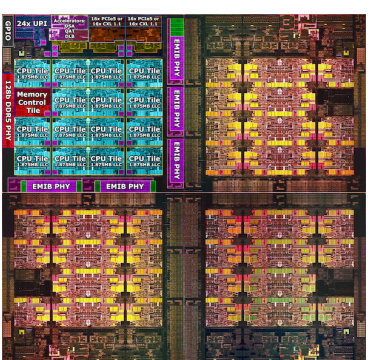


1. Analog View of a Transistor

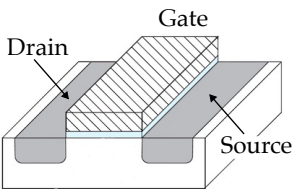
- **Transistors:** Invented by John Bardeen, Walter Brattain, and William Shockley at Bell Labs in 1947
- **Integrated Circuits:** Independently developed by Jack Kilby (at TI) and Robert Noyce (at Fairchild) in the 1950s; Noyce and Gordon Moore founded Intel in 1968

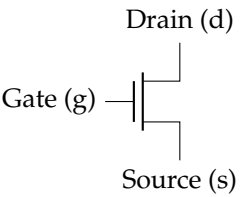


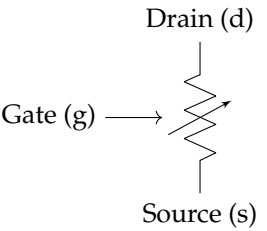
- **Intel Saphire Rapids (2023)**
  - Number of transistors: 61 billion
  - Technology node: Intel 7



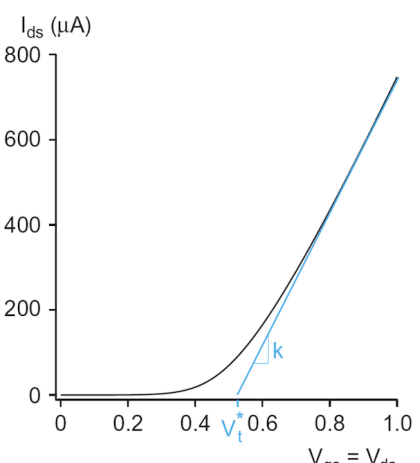
Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)





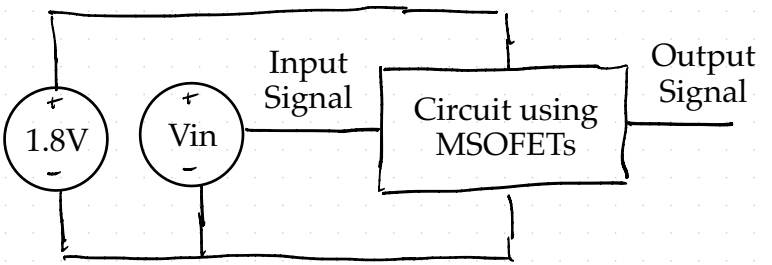


- MOS: Need three materials to make a transistor
  - _____ strong conductor of current
  - _____ insulator (does not conduct)
  - _____ conduction can be controlled
- FET: Electric field causes conduction between source and drain



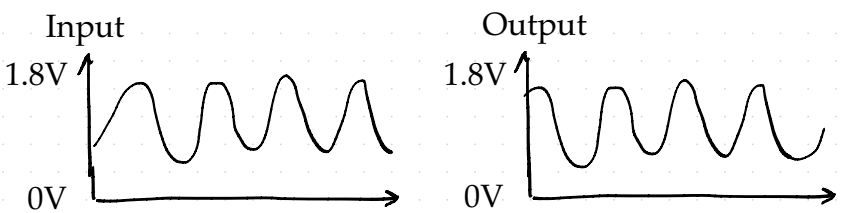
- MOSFET operation
  - As gate voltage increases, current from drain to source also increases
  - At specific threshold voltage, current starts to increase very rapidly
- MOSFET analog applications
  - Various amplifiers
  - Operational amplifiers
  - Current sources and mirrors
  - Voltage-controlled oscillators
  - Voltage regulators
  - Filters

2. Digital View of a Transistor

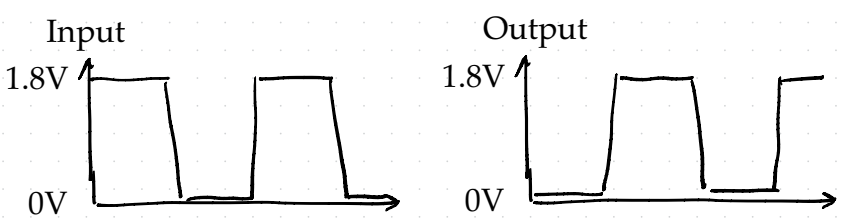


2.1. Digital Abstraction

Analog circuits (continuous values are possible)

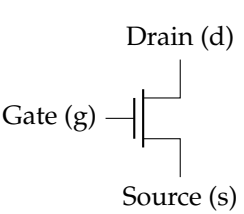


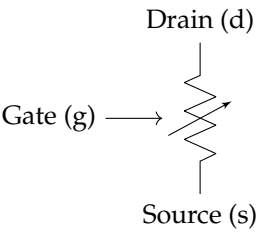
Digital circuits (only two specific values are possible)

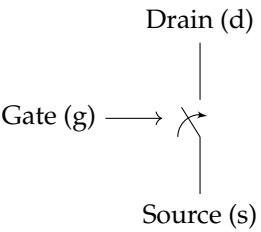


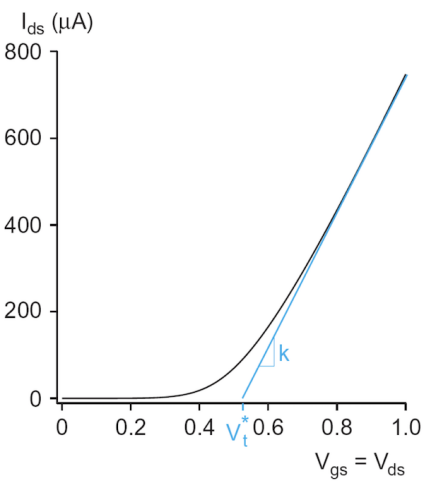
2.2. Switch-Level Model for a Transistor

- Non-linear change in current make transistors act like switches
  - If Vg = 0V, then the switch is open
  - If Vg = 1.8V, then the switch is closed

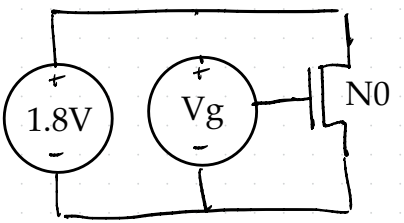


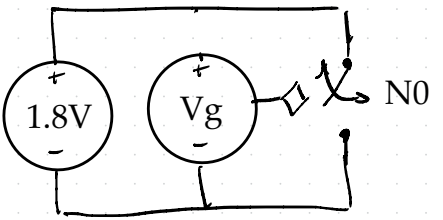




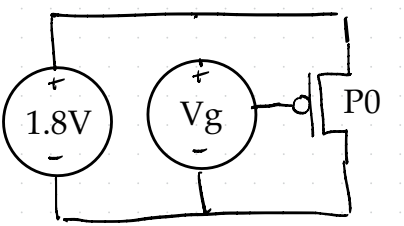


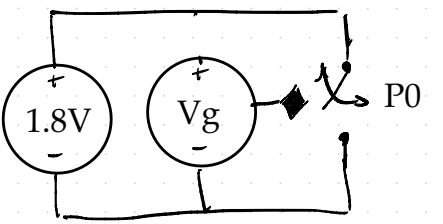
- Two different kinds of MOSFETs
  - **NMOS:** Closed when Vg = 1.8V, open when Vg = 0V
  - **PMOS:** Closed when Vg = 0V, open when Vg = 1.8V





Vg	N0
0V	
1.8V	



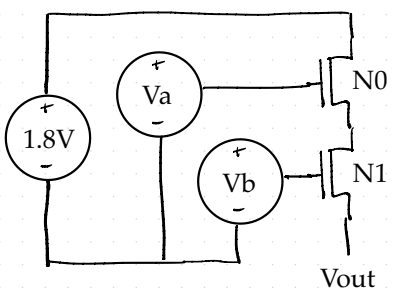


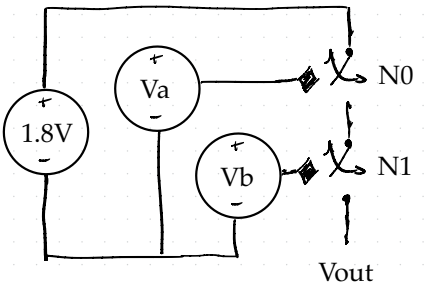
Vg	P0
0V	
1.8V	

- NMOS and PMOS have complementary properties
  - For same input, one will be on and one will be off
  - Digital CMOS circuits combine NMOS and PMOS transistors

2.3. Transistor Networks

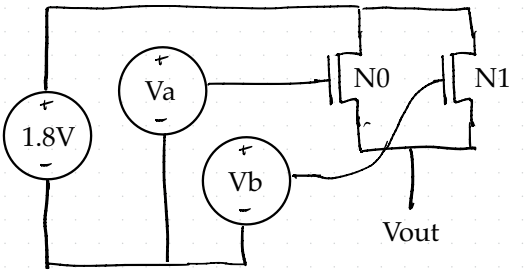
NMOS transistors in series

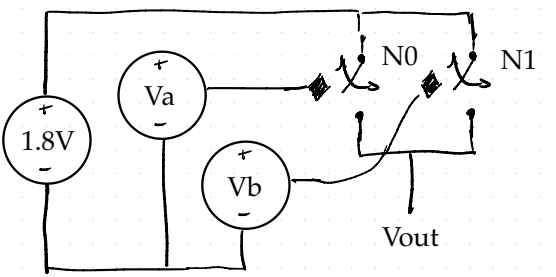




Va	Vb	N0	N1	Vout
0V	0V			
0V	1.8V			
1.8V	0V			
1.8V	1.8V			

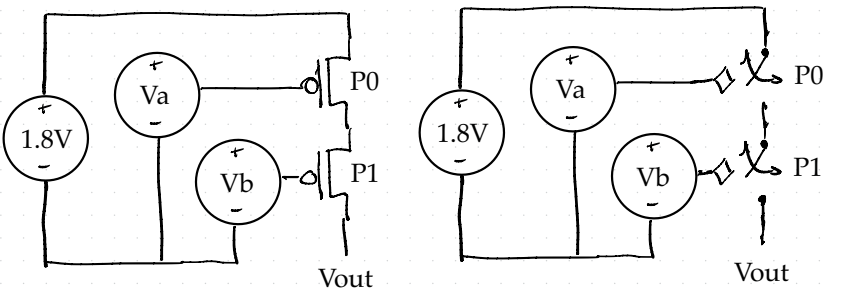
NMOS transistors in parallel





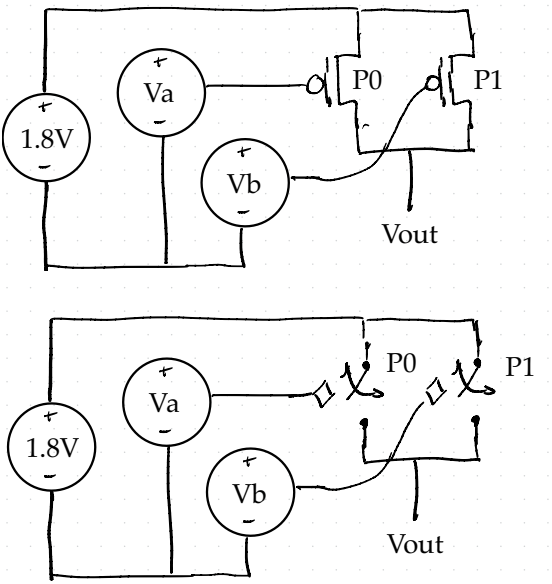
Va	Vb	N0	N1	Vout
0V	0V			
0V	1.8V			
1.8V	0V			
1.8V	1.8V			

PMOS transistors in series



Va	Vb	P0	P1	Vout
0V	0V			
0V	1.8V			
1.8V	0V			
1.8V	1.8V			

PMOS transistors in parallel



Va	Vb	P0	P1	Vout
0V	0V			
0V	1.8V			
1.8V	0V			
1.8V	1.8V			

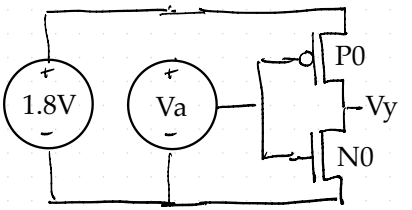
Summary of transistor networks

Va	Vb	NMOS Series Vout	NMOS Parallel Vout	PMOS Series Vout	NMOS Parallel Vout
0V	0V				
0V	1.8V				
1.8V	0V				
1.8V	1.8V				

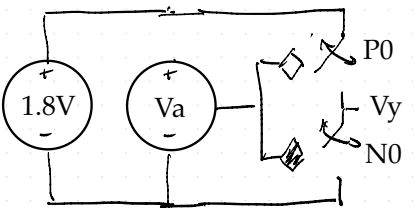
- NMOS and PMOS have complementary properties
  - When NMOS in series are floating, PMOS in parallel are not floating
  - When BMOS in parallel are floating, PMOS in series are not floating
  - Digital CMOS circuits combine NMOS and PMOS transistors

3. CMOS Inverter

Transistor Schematic



Switch-Level Model



Simulation Table

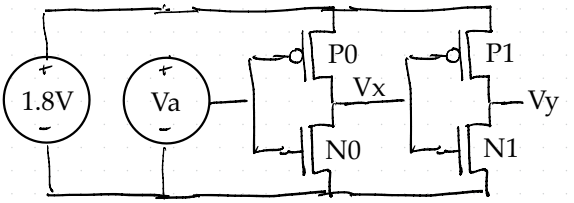
- Illustrates how outputs change over time for given input signals
- Assume all signals propagate with zero delay

Va	P0	N0	Vy
0V			
1.8V			
0V			
1.8V			

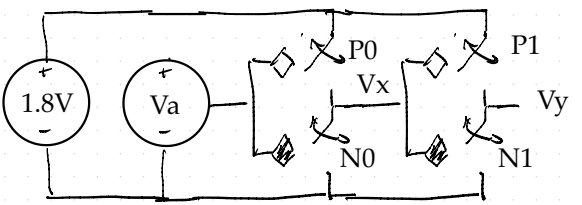
Waveform

- Illustrates how outputs change over time for given input signals
- Various delay models possible (assume constant delay model of 1τ)

Transistor Schematic



Switch-Level Model



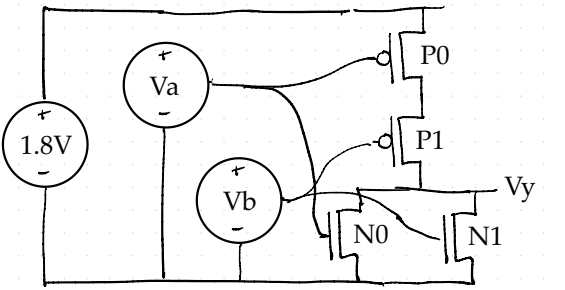
Simulation Table

Va	P0	N0	Vx	P1	N1	Vy
0V						
1.8V						
0V						
1.8V						

Waveform

4. Simple Digital CMOS Circuits

Transistor-Level Schematic

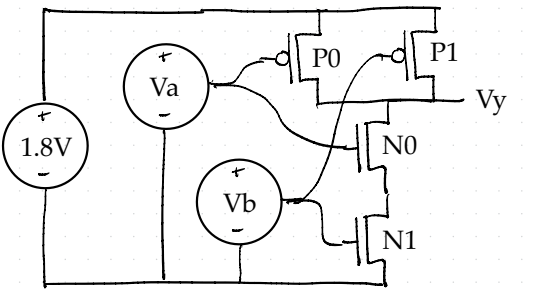


Switch-Level Model

Simulation Table

Va	Vb	P0	P1	N0	N1	Vy
0V	0V					
0V	1.8V					
1.8V	0V					
1.8V	1.8V					

Transistor-Level Schematic

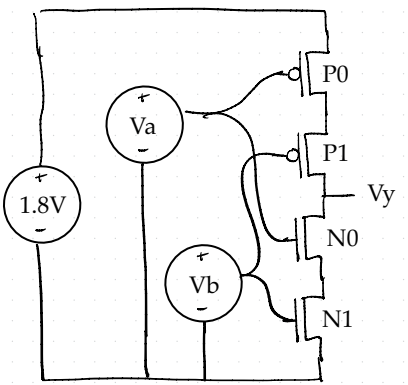


Switch-Level Model

Simulation Table

Va	Vb	P0	P1	N0	N1	Vy
0V	0V					
0V	1.8V					
1.8V	0V					
1.8V	1.8V					

Transistor-Level Schematic



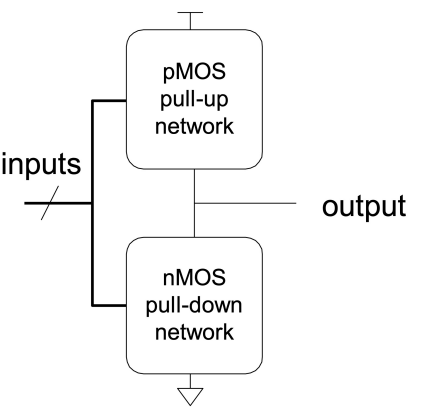
Switch-Level Model

Simulation Table

Va	Vb	P0	P1	N0	N1	Vy
0V	0V					
0V	1.8V					
1.8V	0V					
1.8V	1.8V					

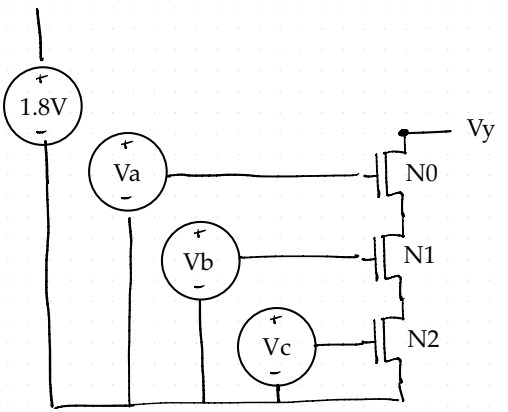
4.1. Rules for Digital CMOS Circuits

- Use NMOS and PMOS transistors such that:
  - The number of PMOS and NMOS transistors are always
  - There should never be a direct path from Vdd to ground
  - The output should never be floating
- Circuit is divided into two parts:
  - Pull-up network exclusively uses PMOS transistors
  - Pull-down network exclusively uses NMOS transistors
- The pull-up and pull-down networks are duals of each other
  - Two transistors in series in the pull-down network will be in parallel in the pull-up network
  - Two transistors in parallel in the pull-down network will be in series in the pull-up network
  - Apply these rules hierarchically to subnets

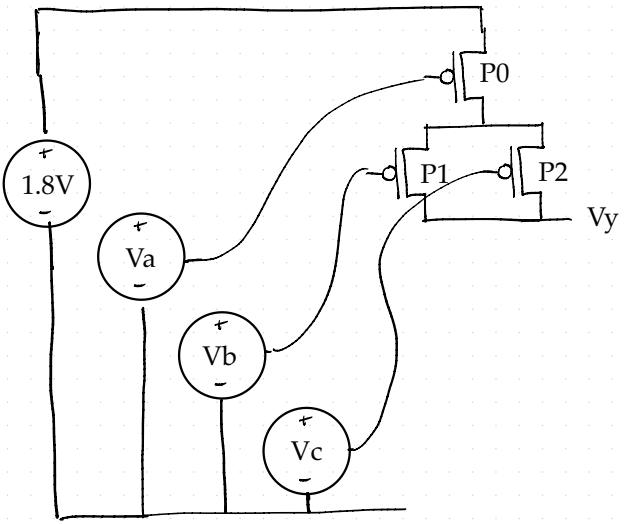


5. More Complex Digital CMOS Circuits

5.1. Multi-Input Digital Circuits

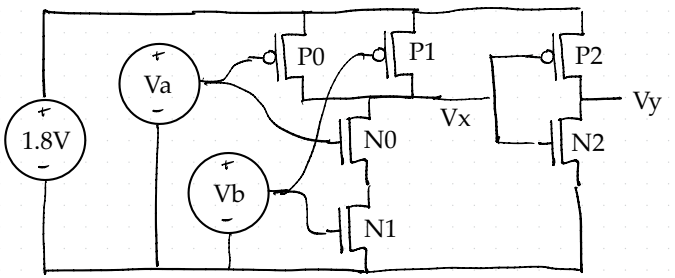


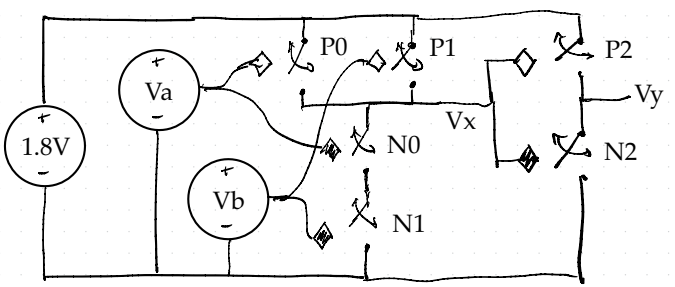
Va	Vb	Vc	P0	P1	P2	N0	N1	N2	Vy
0V	0V	0V							
0V	0V	1.8V							
0V	1.8V	0V							
0V	1.8V	1.8V							
1.8V	0V	0V							
1.8V	0V	1.8V							
1.8V	1.8V	0V							
1.8V	1.8V	1.8V							



Va	Vb	Vc	P0	P1	P2	N0	N1	N2	Vy
0V	0V	0V							
0V	0V	1.8V							
0V	1.8V	0V							
0V	1.8V	1.8V							
1.8V	0V	0V							
1.8V	0V	1.8V							
1.8V	1.8V	0V							
1.8V	1.8V	1.8V							

5.2. Multi-Stage Digital Circuits

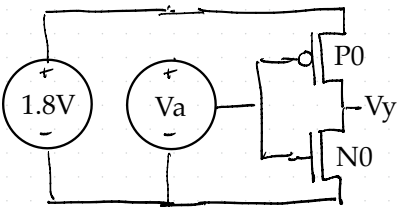




Va	Vb	P0	P1	N0	N1	Vy	P2	N2	Vy
0V	0V								
0V	1.8V								
1.8V	0V								
1.8V	1.8V								

6. Summary of Abstractions

Transistor Schematic



Switch-Level Model