ECE 2300 Digital Logic and Computer Organization Fall 2024

Topic 6: Sequential Logic Gates

School of Electrical and Computer Engineering
Cornell University

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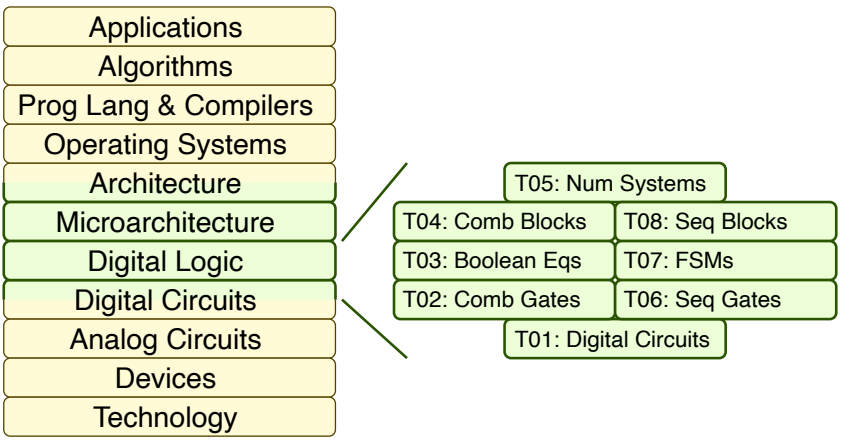
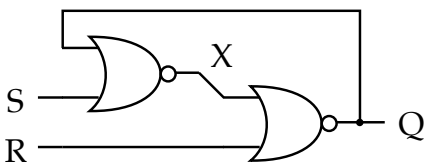


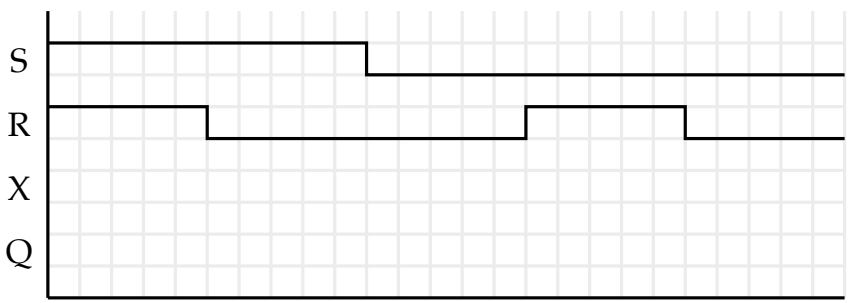
1. Latches, Flip-Flops, and Registers

- *Combinational Logic:* outputs only depend on current inputs
- *Sequential Logic:* outputs depend on current inputs *and previous inputs*

1.1. SR Latch



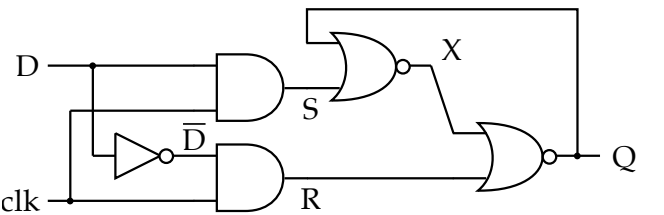
S	*R*	*X*	*Q*
0	0		
0	1		
1	0		
1	1		

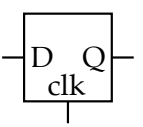


- *SR Latch:* bi-stable state element with set and reset inputs

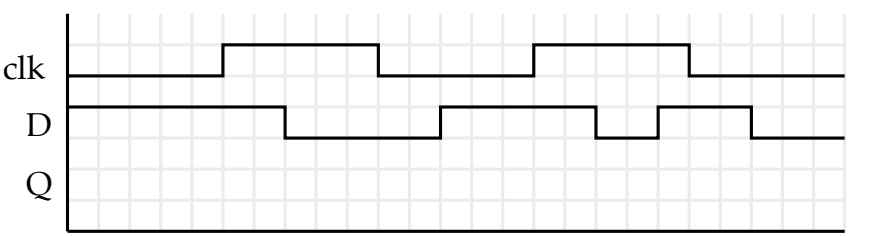
1.2. D Latch

- *SR Latch:* Asserting one input determines not only *what* the new state should be but also *when* it should change
- *D Latch:* One input controls *what* the next state should be, while second input controls *when* the state should change



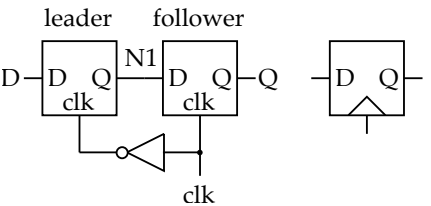


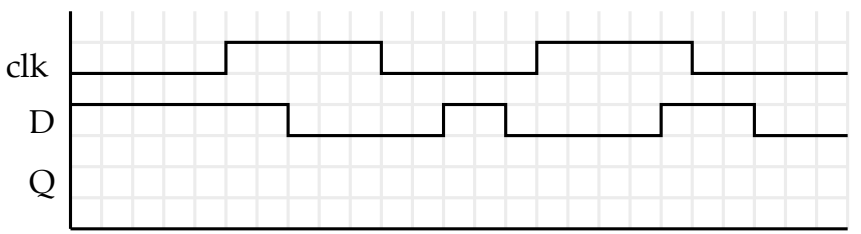
clk	D	$\overline{D}$	S	R	X	Q
0	?					
1	0					
1	1					

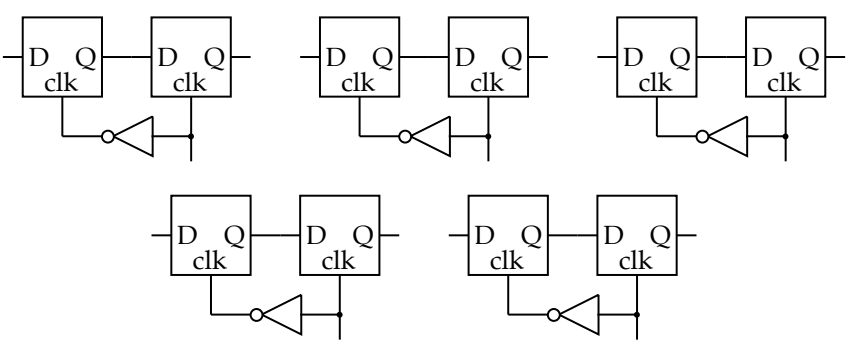


1.3. D Flip-Flop

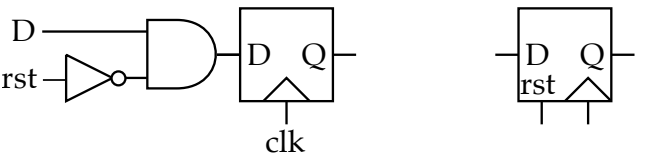
- *D Latch:* Input is *sampled* continuously when clock is high
- *D Flip-Flop:* Input is only *sampled* at a specific instance in time (on the rising edge of the clock)



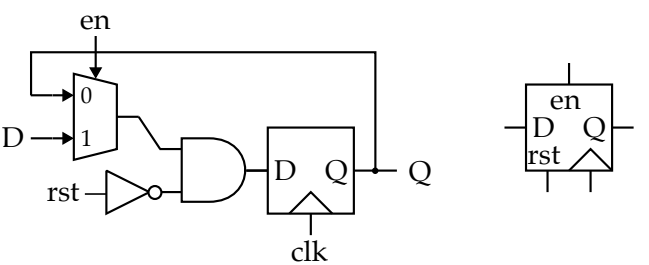




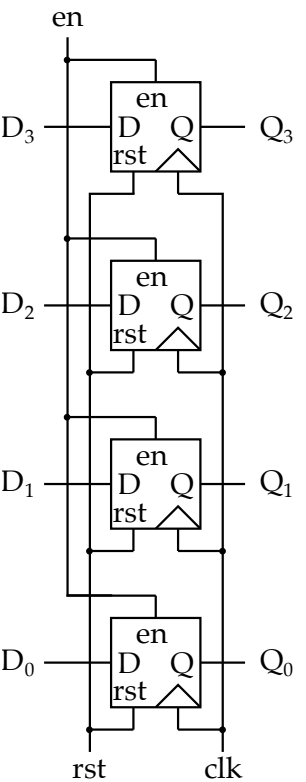
1.4. D Flip-Flop with Reset

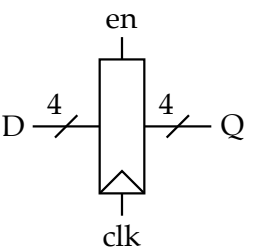


1.5. D Flip-Flop with Reset and Enable

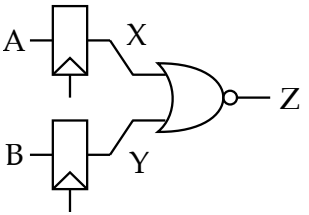


1.6. Multi-Bit Register

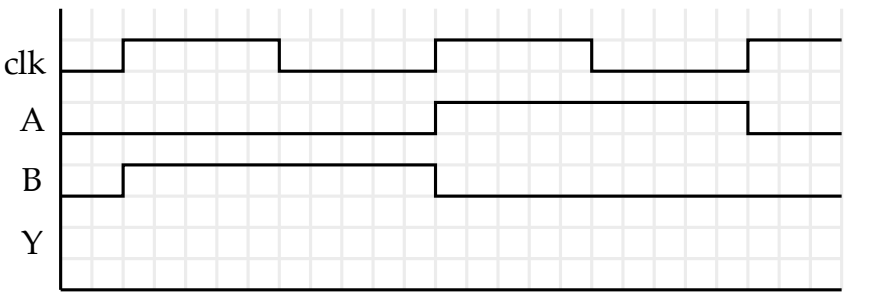




2. Sequential Gate-Level Networks

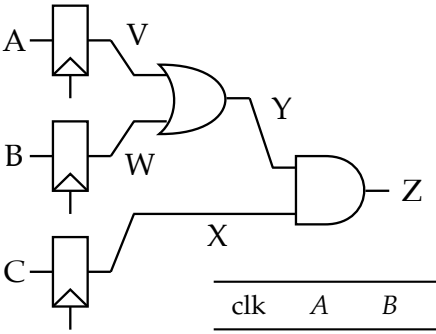


clk	*A*	*B*	*X*	*Y*	*Z*
0	0	0			
1	0	1			
0	0	1			
1	1	0			
0	1	0			
1	0	0			

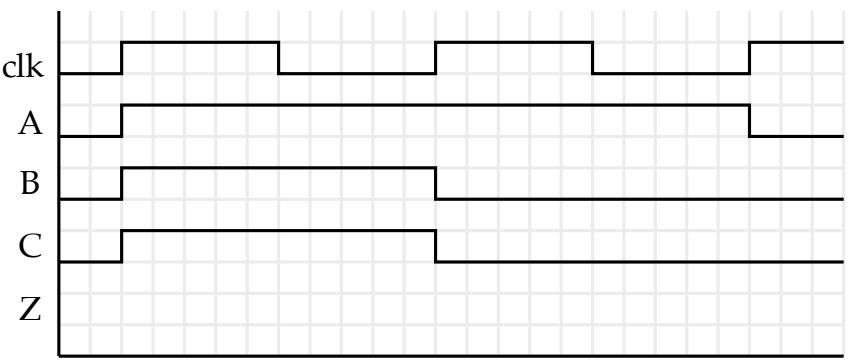


- Convention for tables with implicit clock
  - One row per clock cycle
  - Inputs represent values before the rising edge
  - Other signals represent stable values after the rising edge

A	*B*	*X*	*Y*	*Z*
0	0			
0	1			
1	0			
0	0			



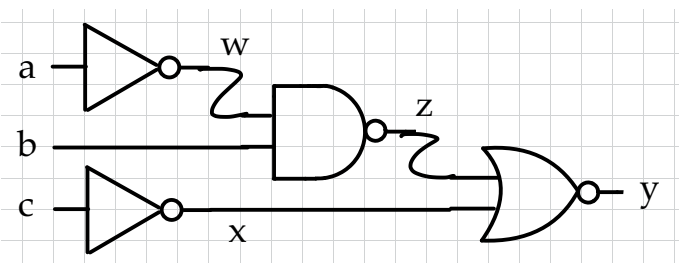
clk	*A*	*B*	*C*	*V*	*W*	*X*	*Y*	*Z*
0	0	0	0					
1	1	1	1					
0	1	1	1					
1	1	0	0					
0	1	0	0					
1	0	0	0					



3. Sequential Gate-Level Timing

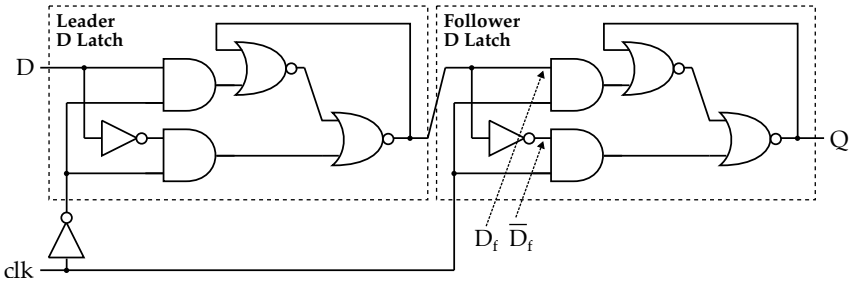
- **Critical Path for Combinational Gate-Level Networks:** longest propagation path delay from any input to any output

Gate	t_{pd}	t_{cd}
NOT	1τ	1τ
NAND2	2τ	1τ
NOR2	3τ	1τ
AND2	3τ	1τ
OR2	4τ	1τ



Path	Propagation Delay	Critical Path?
a → NOT → NAND2 → NOR2 → y		
b → NAND2 → NOR2 → y		
c → NOT → NOR2 → y		

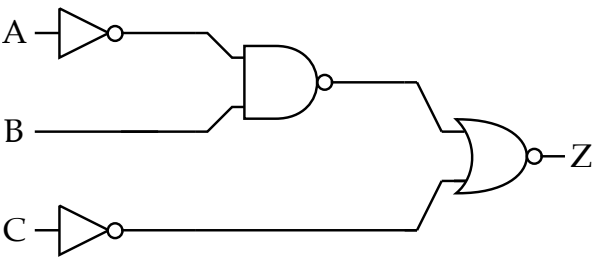
- Identify all paths from any input to any output



Path
D → AND2 → NOR2 → NOR2 → AND2 → NOR2 → NOR2 → Q

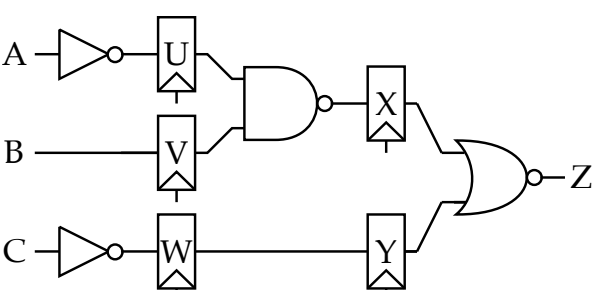
Critical Path for Combinational Gate-Level Networks

- Longest propagation path delay from:
  - any input to any output

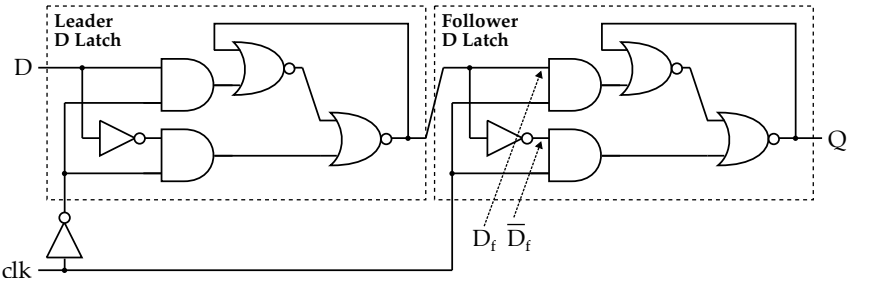


Critical Path for Sequential Gate-Level Networks

- Longest propagation path delay from:
  - any input to any output
  - any input to any flip-flop
  - any flip-flop to any flip-flop
  - any flip-flop to any output

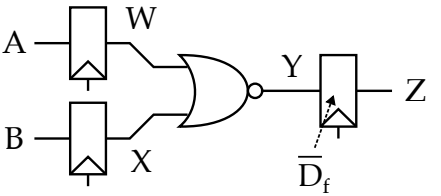


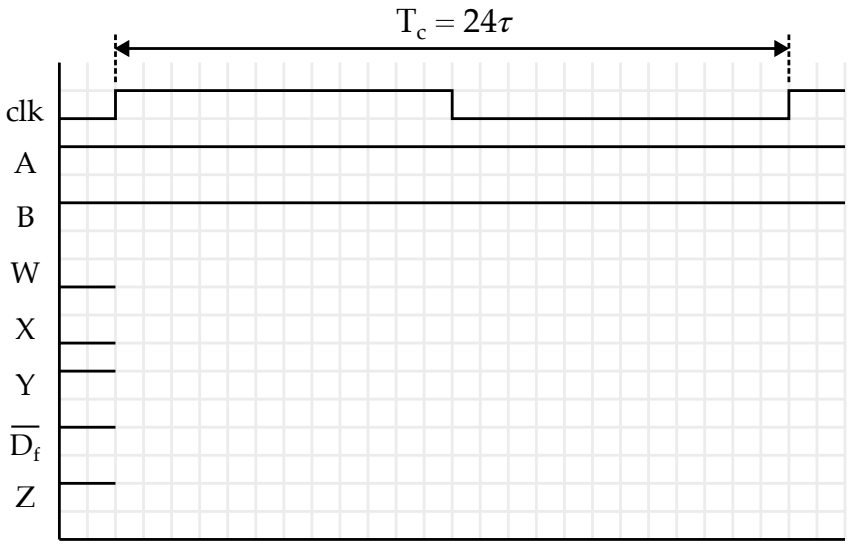
3.1. Setup Time Constraint

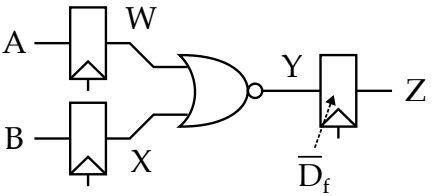


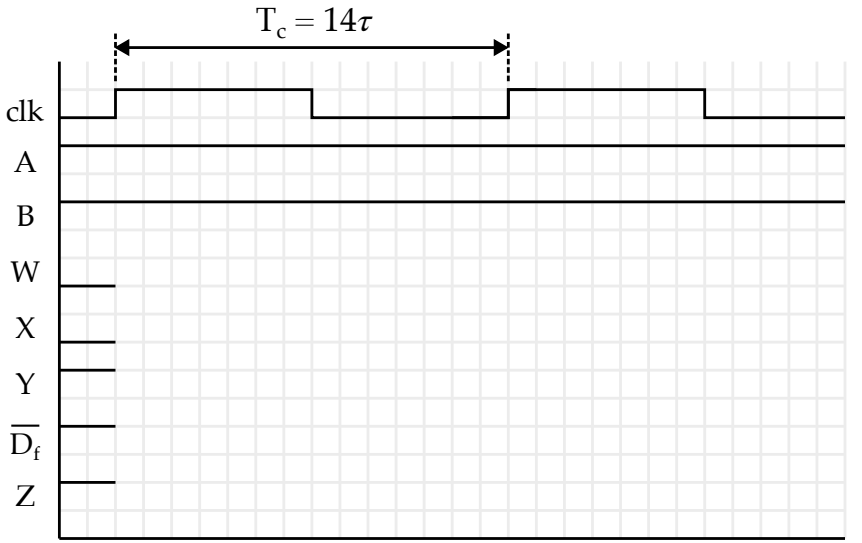
Clock-to-Q Propagation Delay ($t_{pd,cq}$)

Setup Time (t_{setup})


A
W
B
X
Y
Z
$\overline{D}_f$

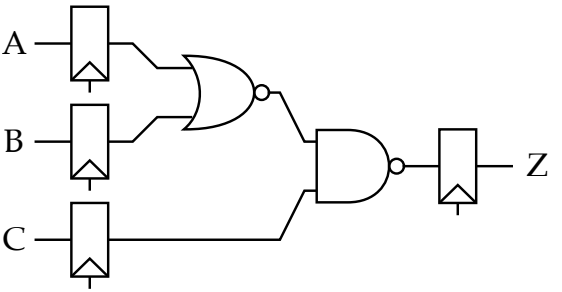

$T_c = 24\tau$
clk
A
B
W
X
Y
$\overline{D}_f$
Z





Setup Time Constraint or Max-Delay Constraint

Consider the following sequential gate-level network.

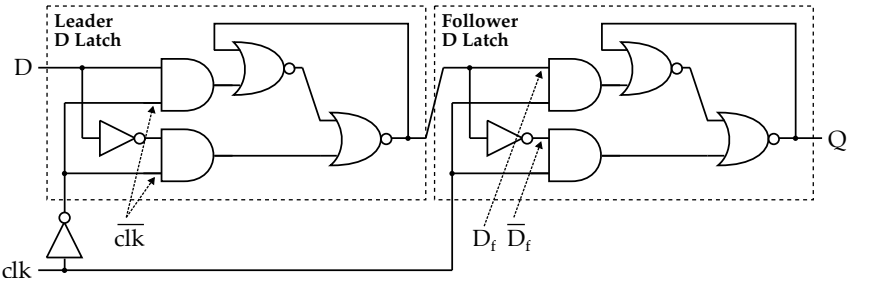


Highlight the critical path on the above gate-level network. Use the setup time constraint to derive an equation for the minimum clock period or cycle time (T_c) in terms of the following parameters.

- Flip-flop clock-to-Q propagation delay ($t_{pd,cq}$)
- Flip-flop setup time (t_{setup})
- Propagation delay of NOR2 ($t_{pd,nor2}$)
- Propagation delay of NAND2 ($t_{pd,nand2}$)

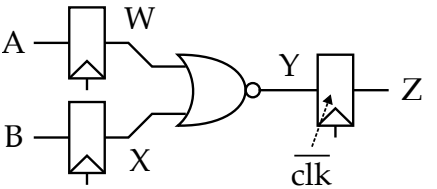
Calculate the minimum clock period or cycle time (T_c) given the delay model we have developed in this topic.

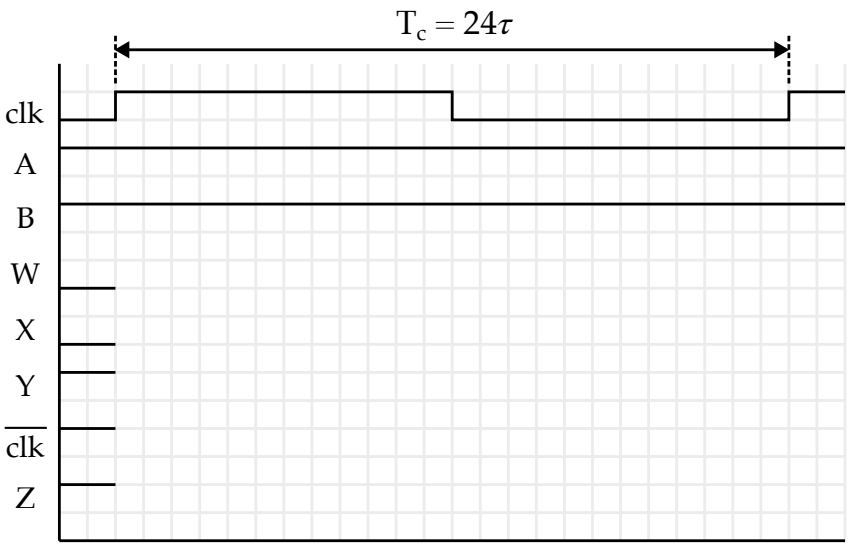
3.2. Hold Time Constraint

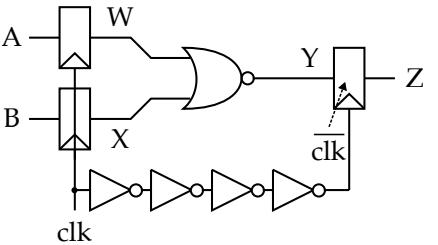


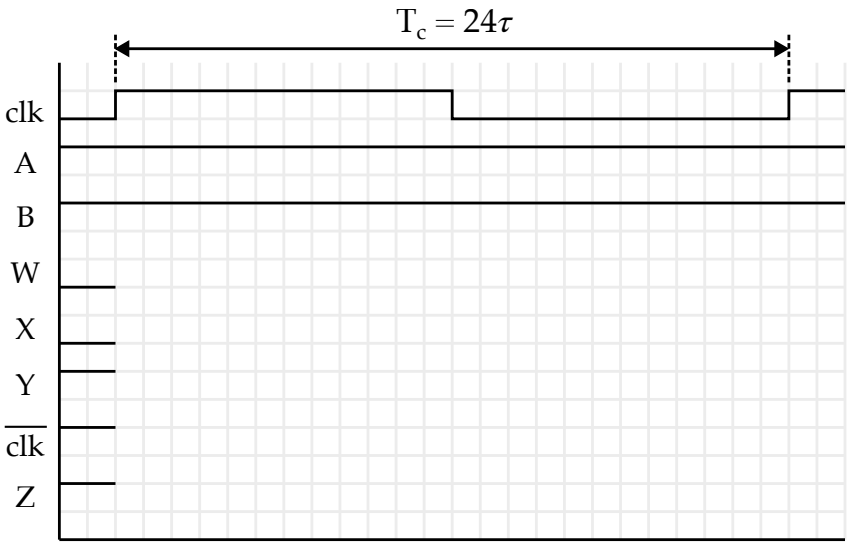
Clock-to-Q Contamination Delay ($t_{cd,cq}$)

Hold Time (t_{hold})


A
W
B
X
Y
Z
clk


$T_c = 24\tau$
clk
A
B
W
X
Y
clk
Z





Hold Time Constraint or Min-Delay Constraint

3.3. Summary of Sequential Gate-Level Timing