ECE 2300 Digital Logic and Computer Organization

Topic 6: Sequential Logic

`http://www.csl.cornell.edu/courses/ece2300`
School of Electrical and Computer Engineering
Cornell University

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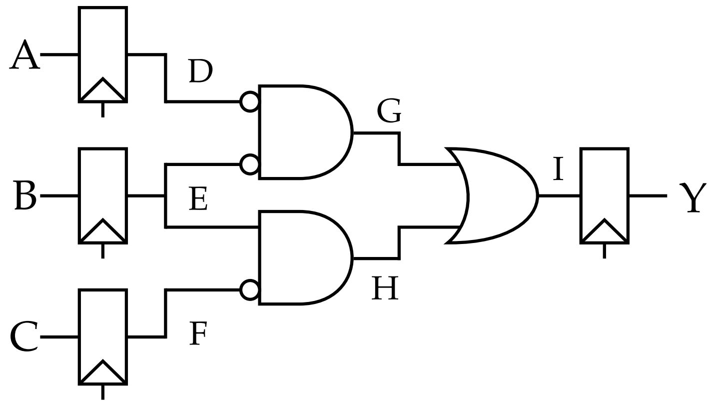
List of Problems

Problem 1. Sequential Network 1

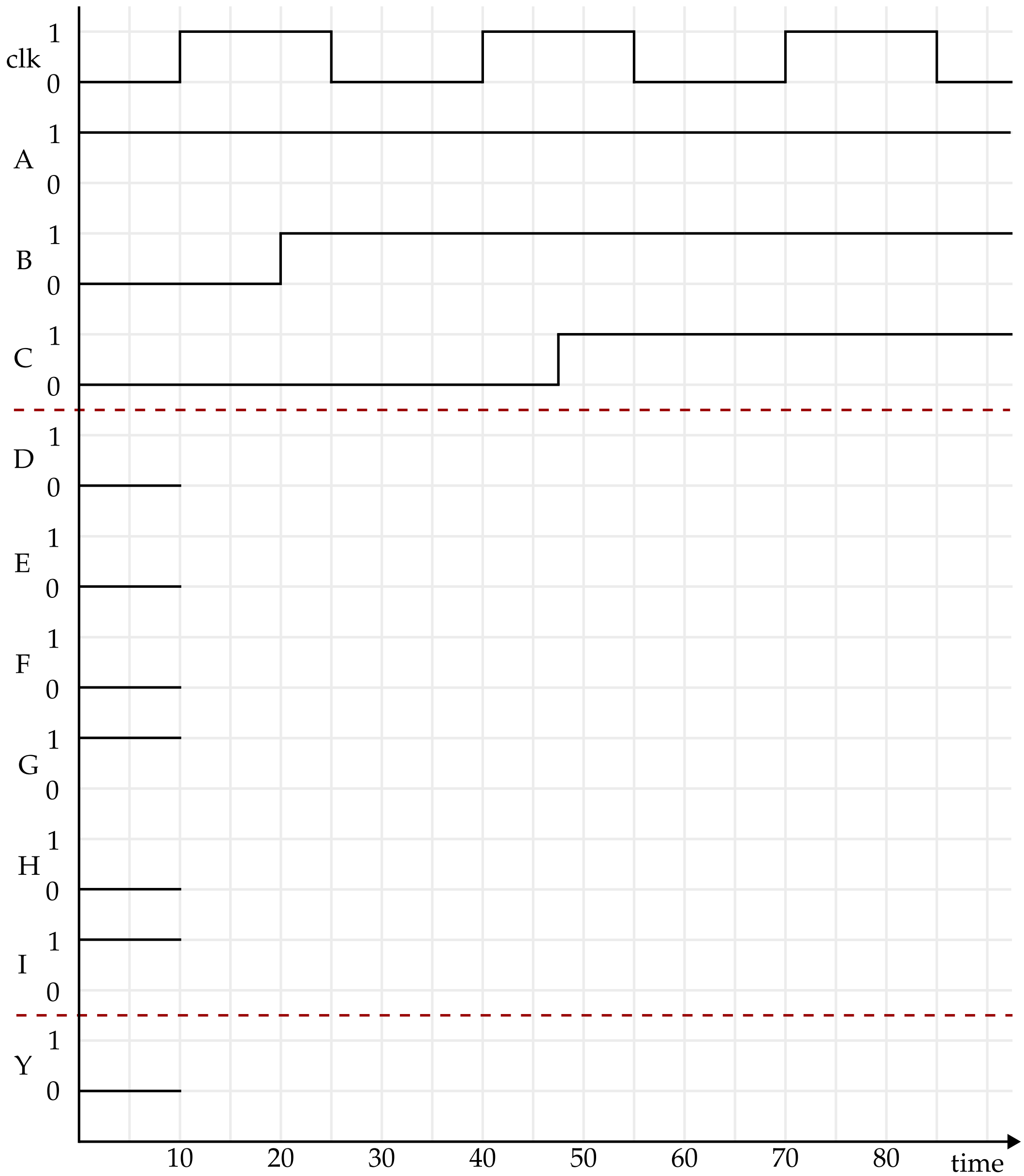
Complete the explicit-clock simulation table for the following sequential network.



clk	A	B	C	D	E	F	G	H	I	Y
1	0	0	0							
0	0	0	0							
1	1	0	0							
0	1	0	0							
1	1	1	0							
0	1	1	0							
1	1	1	1							
0	1	1	1							
1	0	0	1							
0	0	0	1							
1	0	0	0							
0	0	0	0							

	t_{pd}	t_{cd}
NOT	1τ	1τ
AND2	3τ	1τ
OR2	4τ	1τ
FF (t_{cq})	9τ	2τ
FF (t_{setup})	10τ	
FF (t_{hold})	1τ	
T_C	30τ	

Complete the timing diagram for the sequential gate network utilizing the delay model to the right. Illustrate both the propagation and contamination delays in the timing diagram. *Note: Use NOT-Gates for inverted inputs.*



Prof. Batten's Solution

`https://vod.video.cornell.edu/media/t/1_uh9aao0s`

Use the following table to list every constraint which must be satisfied to ensure correct operation of this gate-level network. Start by labeling the two possible constraints at the top of the table. You do not need to include the unit τ in your constraints. Each path should be specified with just the start and end points of the path. You do not need to list the gates along the path. Assume paths that start at an input port or end at an output port are unconstrained. Each constraint should be expressed as an inequality. If the constraint is satisfied use $\geq$ or $\leq$. If the constraint is not satisified use $\ngeq$ or $\nleq$. **You must show each delay component in the inequality along with the the final sum. Circle any constraints which are not statisified and would result in a timing violation.** *Note: Use NOT-Gates for inverted inputs.*

Path Start Point	Path End Point	____________ Constraint	____________ Constraint

Are there any unsatisfied constraints (i.e., timing violations)?

Identify the critical path. Describe its path and calculate its setup time slack.

Identify the short path. Describe its path and calculate its hold time slack.

What is the minimum clock period (T_C) that would still ensure correct operation?

What is the maximum clock frequency that would still ensure correct operation? Presume 1τ to be 1 ns.

Computing Slack

Slack measures the margin by which the timing constraints are met (positive slack) or missed (negative slack). For the setup constraint ($T_C \geq t_{pd,cq} + t_{pd,comb} + t_{setup}$), the setup slack is computed using the following formula:

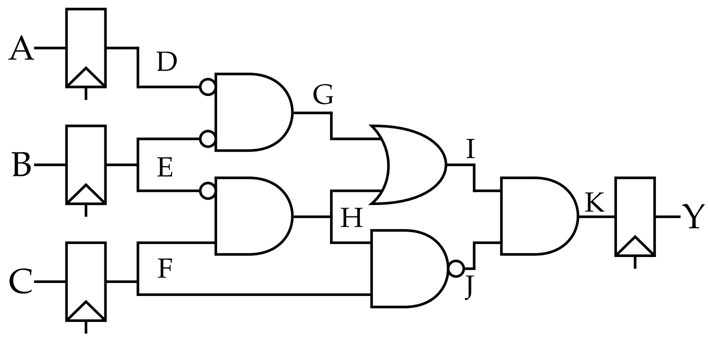
$$t_{slack,setup} = T_C - t_{pd,cq} - t_{pd,comb} - t_{setup}$$

For the hold constraint ($t_{hold} \leq t_{cd,cq} + t_{cd,comb}$), the hold slack is computed using the following formula:

$$t_{slack,hold} = t_{cd,cq} + t_{cd,comb} - t_{hold}$$

Problem 2. Sequential Network 2

Complete the implicit-clock simulation table for the following sequential network. *Note: Due to the logic in the subsequent stage, a larger output flip-flop is used in this stage (with different setup and hold parameters).*



A	B	C	D	E	F	G	H	I	J	K	Y
0	0	0									
0	1	1									
0	1	0									
1	1	1									

Use the following table to list every constraint which must be satisfied to ensure correct operation of this gate-level network. Start by labeling the two possible constraints at the top of the table. You do not need to include the unit τ in your constraints. Each path should be specified with just the start and end points of the path. You do not need to list the gates along the path. Assume paths that start at an input port or end at an output port are unconstrained. Each constraint should be expressed as an inequality. If the constraint is satisfied use $\geq$ or $\leq$. If the constraint is not satisified use $\not\geq$ or $\not\leq$. **You must show each delay component in the inequality along with the the final sum. Circle any constraints which are not statisified and would result in a timing violation.**

	t_{pd}	t_{cd}
NOT	1τ	1τ
NAND2	2τ	1τ
AND2	3τ	1τ
OR2	4τ	1τ
FF (t_{cq})	9τ	2τ

FF-Input ($t_{in,setup}$)	10τ
FF-Input ($t_{in,hold}$)	1τ
FF-Output ($t_{out,setup}$)	20τ
FF-Output ($t_{out,hold}$)	5τ
T_C	45τ

Path Start Point	Path End Point	____________ Constraint	____________ Constraint

Are there any unsatisfied constraints (i.e., timing violations)?

Identify the critical path. Describe its path and calculate its setup time slack.

Identify the short path. Describe its path and calculate its hold time slack.

What is the minimum clock period (T_C) and the maximum clock frequency that would still ensure correct operation? Presume 1τ to be 1 ns.

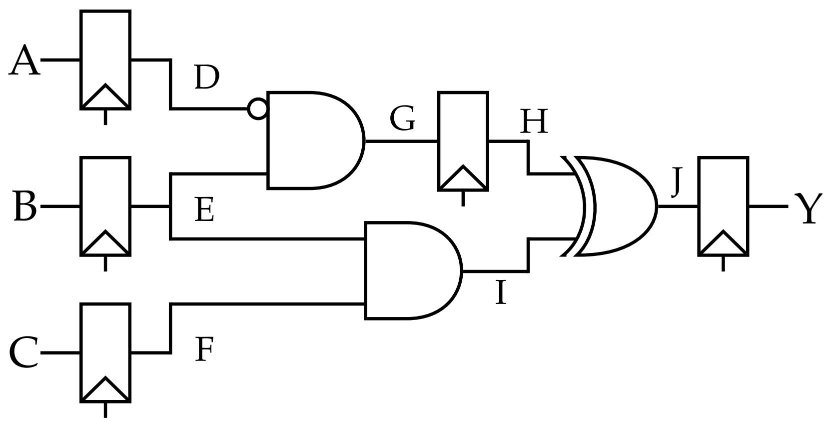
In case the hold constraint was violated: How can this be fixed? Can this fix be performed after tapeout? *Note: Draw the potential fix in the block diagram.*

Stephen's Solution

`https://vod.video.cornell.edu/media/ECE+2300+Topic+6%2C+Practice+Problem+2/1_vvqvf4my`

Problem 3. Sequential Network 3

Complete the implicit-clock simulation table for the following sequential network.



A	B	C	D	E	F	G	H	I	J	Y
0	0	0								
0	1	0								
1	1	0								
1	1	0								
0	1	1								
0	1	1								
1	1	1								
0	1	0								

	t_{pd}	t_{cd}
NOT	1τ	1τ
AND2	3τ	1τ
XOR2	7τ	1τ
FF (t_{cq})	9τ	2τ
FF (t_{setup})	10τ	
FF (t_{hold})	1τ	
T_C	27τ	

Use the following table to list every constraint which must be satisfied to ensure correct operation of this gate-level network. Start by labeling the two possible constraints at the top of the table. You do not need to include the unit τ in your constraints. Each path should be specified with just the start and end points of the path. You do not need to list the gates along the path. Assume paths that start at an input port or end at an output port are unconstrained. Each constraint should be expressed as an inequality. If the constraint is satisfied use $\geq$ or $\leq$. If the constraint is not satisified use $\ngeq$ or $\nleq$. **You must show each delay component in the inequality along with the the final sum. Circle any constraints which are not statisified and would result in a timing violation.** *Note: Use NOT-Gates for inverted inputs.*

Path Start Point	Path End Point	____________ Constraint	____________ Constraint

Are there any unsatisfied constraints (i.e., timing violations)?

Identify the critical path. Describe its path and calculate its setup time slack.

Identify the short path. Describe its path and calculate its hold time slack.

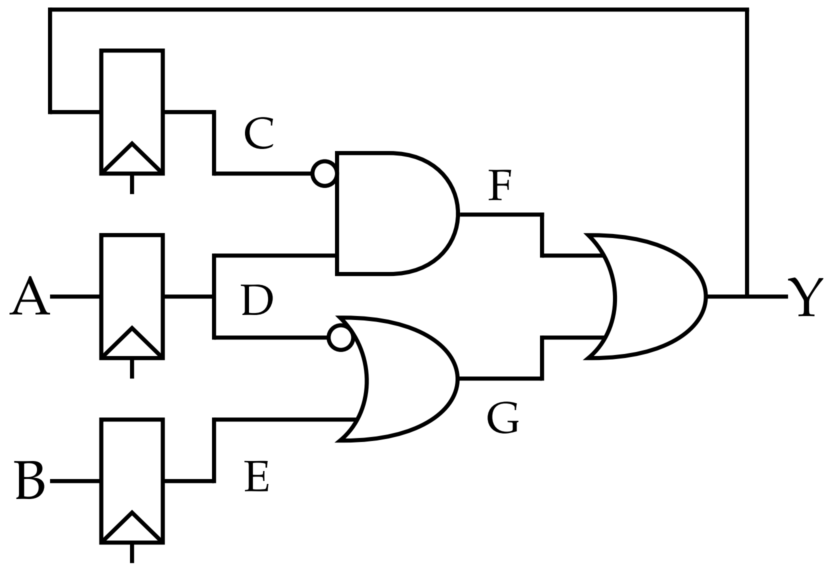
In case the setup constraint was violated: How can this be fixed post-tapeout? Would this lead to a performance degradation?

In case the setup constraint was violated: How can this be fixed pre-tapeout? Would this lead to a performance degradation? What issue could arise? Draw the potential fix in the block diagram.
Note: Ignore potential impact on subsequent logic stages.

Which approach to fix a setup constraint violation would you choose? Why?

Problem 4. Sequential Network 4

Complete the implicit-clock simulation table for the following sequential network.



A	B	C	D	E	F	G	Y
0	0						
1	0						
1	0						
1	1						
0	0						

	t_{pd}	t_{cd}
NOT	1τ	1τ
AND2	3τ	1τ
OR2	4τ	1τ
FF (t_{cq})	9τ	2τ
FF (t_{setup})	10τ	
FF (t_{hold})	1τ	
T_C	30τ	

Use the following table to list every constraint which must be satisfied to ensure correct operation of this gate-level network. Start by labeling the two possible constraints at the top of the table. You do not need to include the unit τ in your constraints. Each path should be specified with just the start and end points of the path. You do not need to list the gates along the path. Assume paths that start at an input port or end at an output port are unconstrained. Each constraint should be expressed as an inequality. If the constraint is satisfied use $\geq$ or $\leq$. If the constraint is not satisified use $\ngeq$ or $\nleq$. **You must show each delay component in the inequality along with the the final sum. Circle any constraints which are not statisified and would result in a timing violation.** *Note: Use NOT-Gates for inverted inputs.*

Path Start Point	Path End Point	____________ Constraint	____________ Constraint

Are there any unsatisfied constraints (i.e., timing violations)?

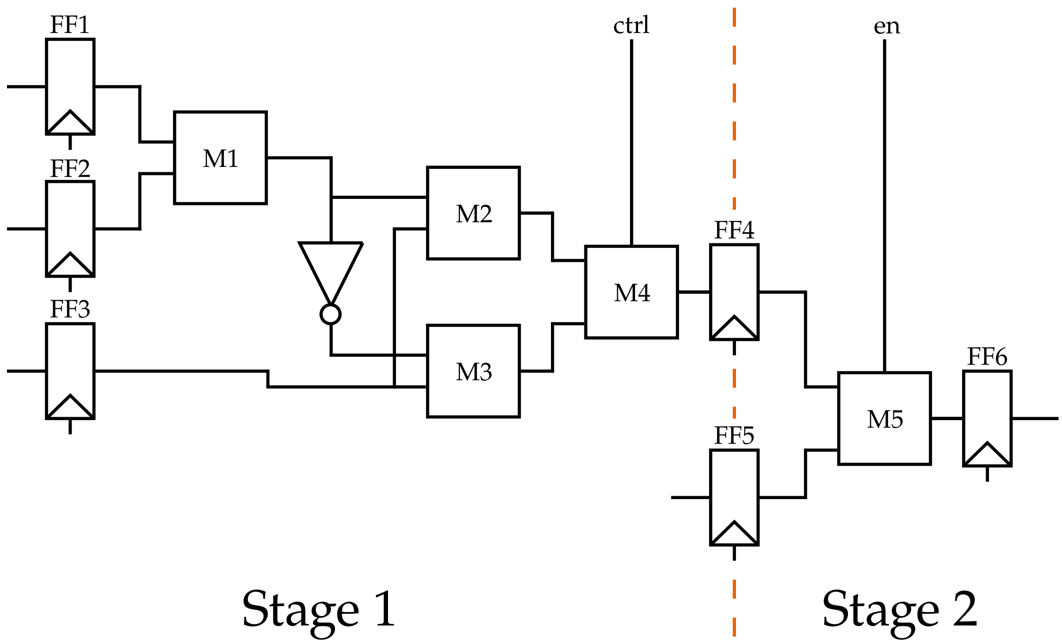
Identify the critical path. Describe its path and calculate its setup time slack.

Identify the short path. Describe its path and calculate its hold time slack.

What is the minimum clock period (T_C) that would still ensure correct operation? What is the maximum clock frequency that would still ensure correct operation? Presume 1τ to be 1 ns.

Problem 5. Sequential Network 5

In this problem, we will inspect a two stage network containing the abstract combinational modules M1-M5.



Use the following table to list every constraint which must be satisfied to ensure correct operation of this gate-level network. Start by labeling the two possible constraints at the top of the table. You do not need to include the unit τ in your constraints. Each path should be specified with just the start and end points of the path. You do not need to list the gates along the path. Assume paths that start at an input port or end at an output port are unconstrained. Each constraint should be expressed as an inequality. If the constraint is satisfied use $\geq$ or $\leq$. If the constraint is not satisified use $\ngeq$ or $\nleq$. **You must show each delay component in the inequality along with the the final sum. Circle any constraints which are not statisified and would result in a timing violation.**

	t_{pd}	t_{cd}
NOT	1τ	1τ
M1	5τ	1τ
M2	10τ	1τ
M3	12τ	1τ
M4	7τ	1τ
M5	17τ	1τ
FF (t_{cq})	9τ	2τ

FF (t_{setup})	10τ
FF (t_{hold})	1τ
T_C	40τ

Path Start Point	Path End Point	____________ Constraint	____________ Constraint

Are there any unsatisfied constraints (i.e., timing violations)?

Identify the critical path. Describe its path and calculate its setup time slack.

Identify the short path. Describe its path and calculate its hold time slack.

Inspect the critical path of the first stage and second stage. How could this network be modified to still meet timing for a clock period of 40τ by exploiting the difference in critical path delays between both stages? Draw the changes in the block diagram.

Write the resulting setup constraint for the first and second stage. Include the useful clock skew in your formulas. Prove that you are meeting timing now.