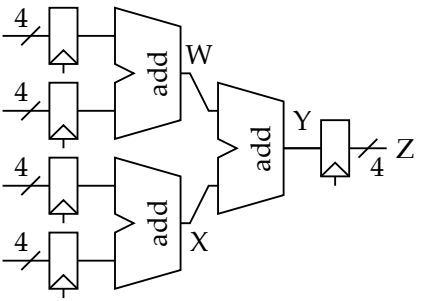
5.4. Tree-Based Quad Adders



Area

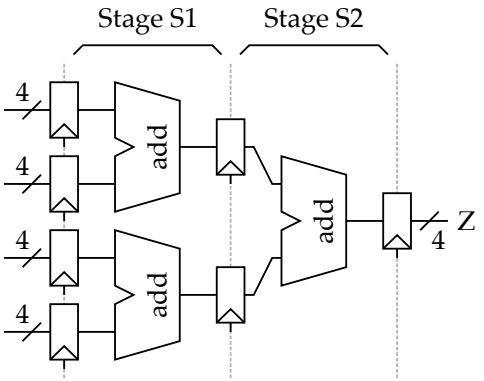
Time/Cycle

Simulation Table

Cycle	Input	After Reg	W	X	Y	Z
0	3, 1, 2, 0					
1	5, 4, 0, 6					
2	4, 5, 3, 1					
3	2, 3, 5, 4					
4						
5						

Transaction Diagram

	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Transaction A														
Transaction B														
Transaction C														
Transaction D														



Area

Time/Cycle

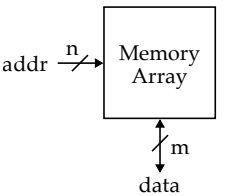
Simulation Table

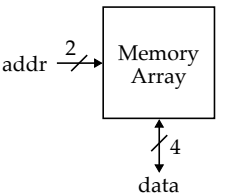
Cycle	Input	Stage S1	Stage S2	Stage S3	Z
0	3, 1, 2, 0				
1	5, 4, 0, 6				
2	4, 5, 3, 1				
3	2, 3, 5, 4				
4					

Transaction Diagram

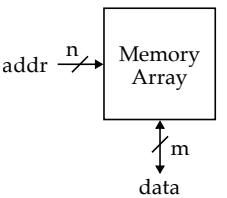
	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Transaction A														
Transaction B														
Transaction C														
Transaction D														

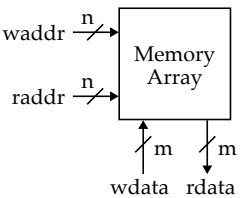
6. Memory Arrays

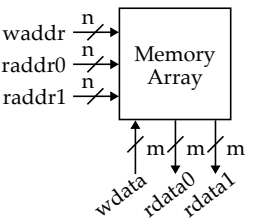


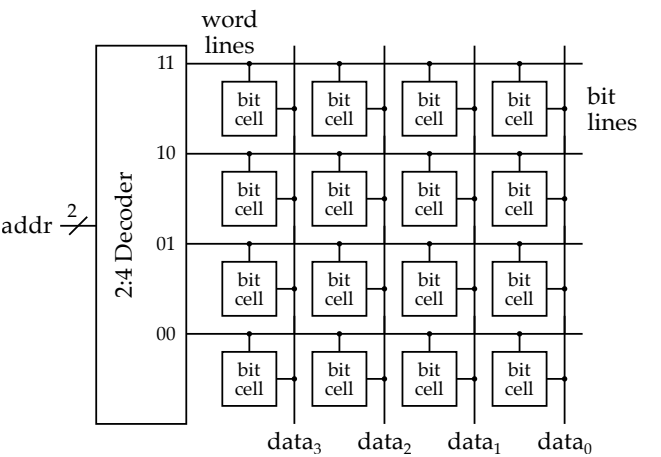


addr	data			
11	0	1	1	0
10	0	0	1	1
01	1	1	0	0
00	1	0	0	0

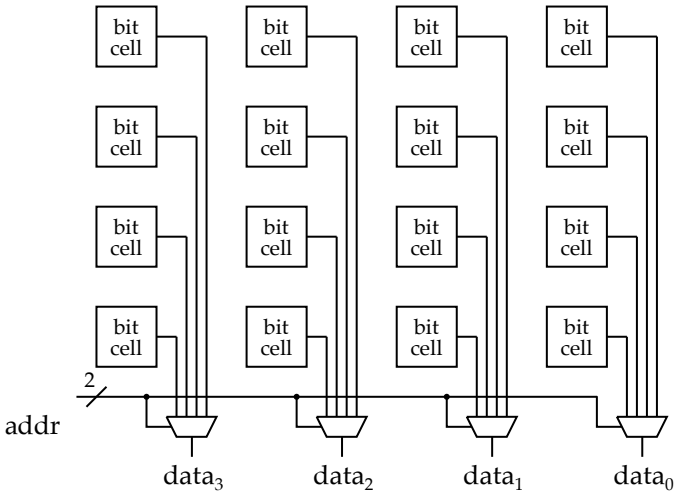




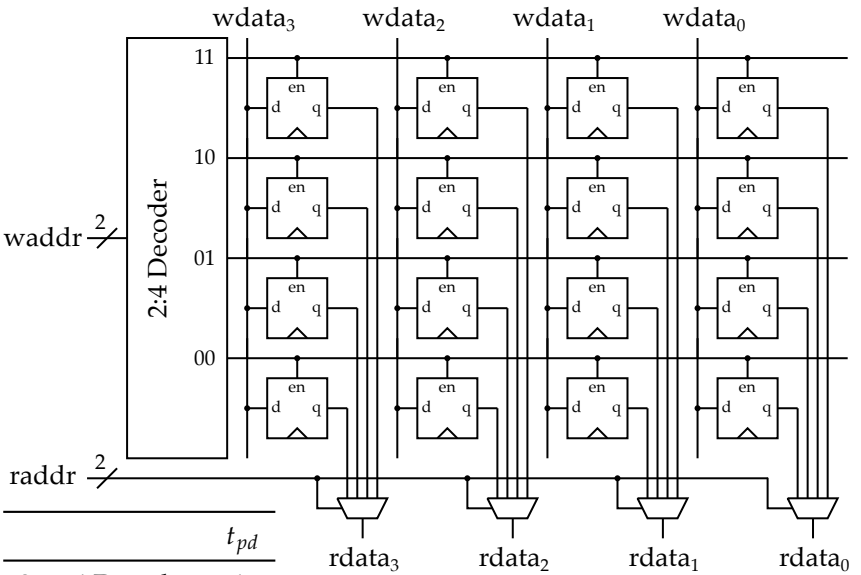




6.1. Read-Only Memories



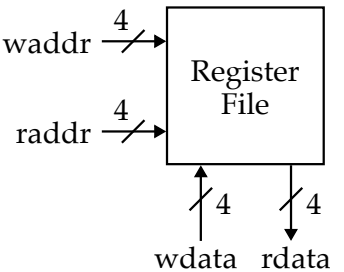
6.2. Register Files



	t_{pd}
2-to-4 Decoder	4τ
1-bit 4-to-1 Mux	10τ
FF (t_{cq})	9τ
FF ($t_{d,setup}$)	10τ
FF ($t_{en,setup}$)	8τ

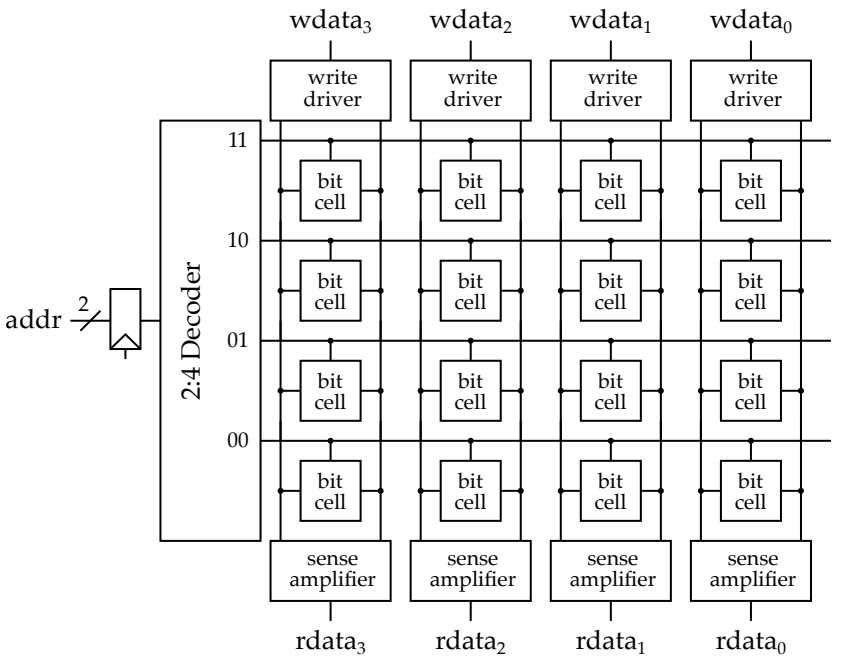
Path	**Propagation Delay**

- We can build a delay model of a register file and then use this model when analyzing more complex hardware designs

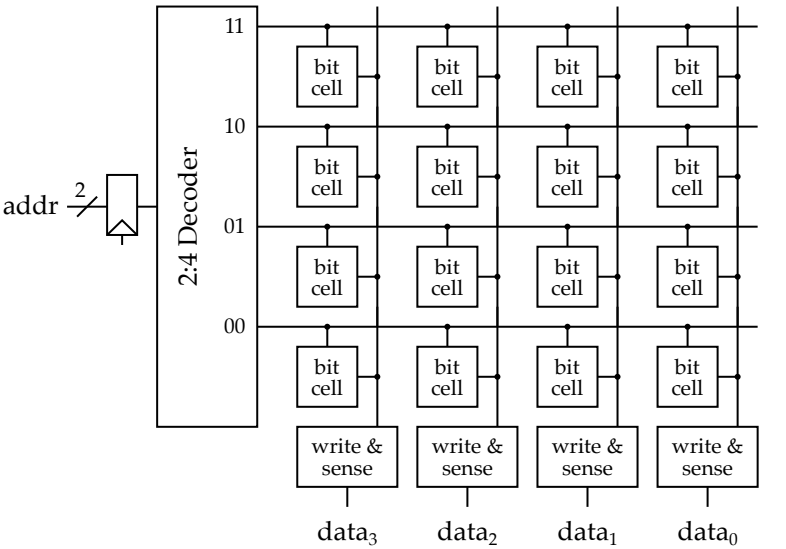


4×4b Reg File ($t_{pd,cq}$)
4×4b Reg File ($t_{pd,read}$)
4×4b Reg File (t_{setup})

6.3. Static Random Access Memories (SRAM)



6.4. Dynamic Random Access Memories (DRAM)



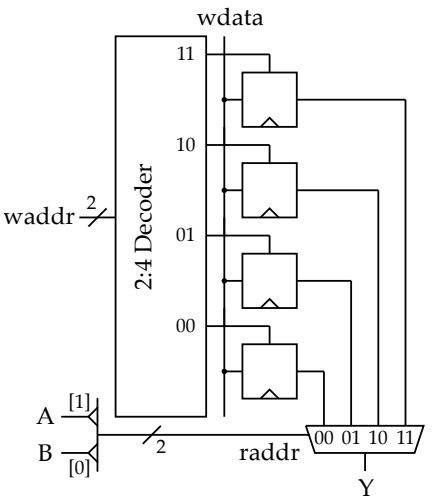
6.5. Comparing Memory Arrays

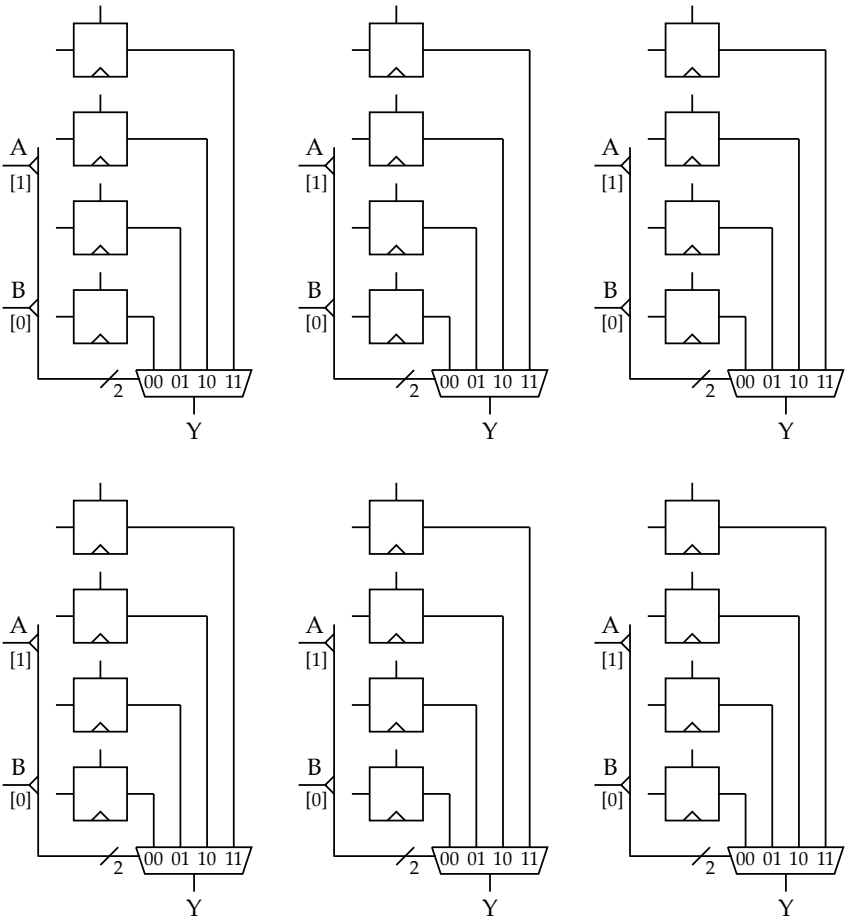
Memory Type	Transistors per Bit Cell	Density	Latency
Register File			
SRAM			
DRAM			

7. Programmable Logic

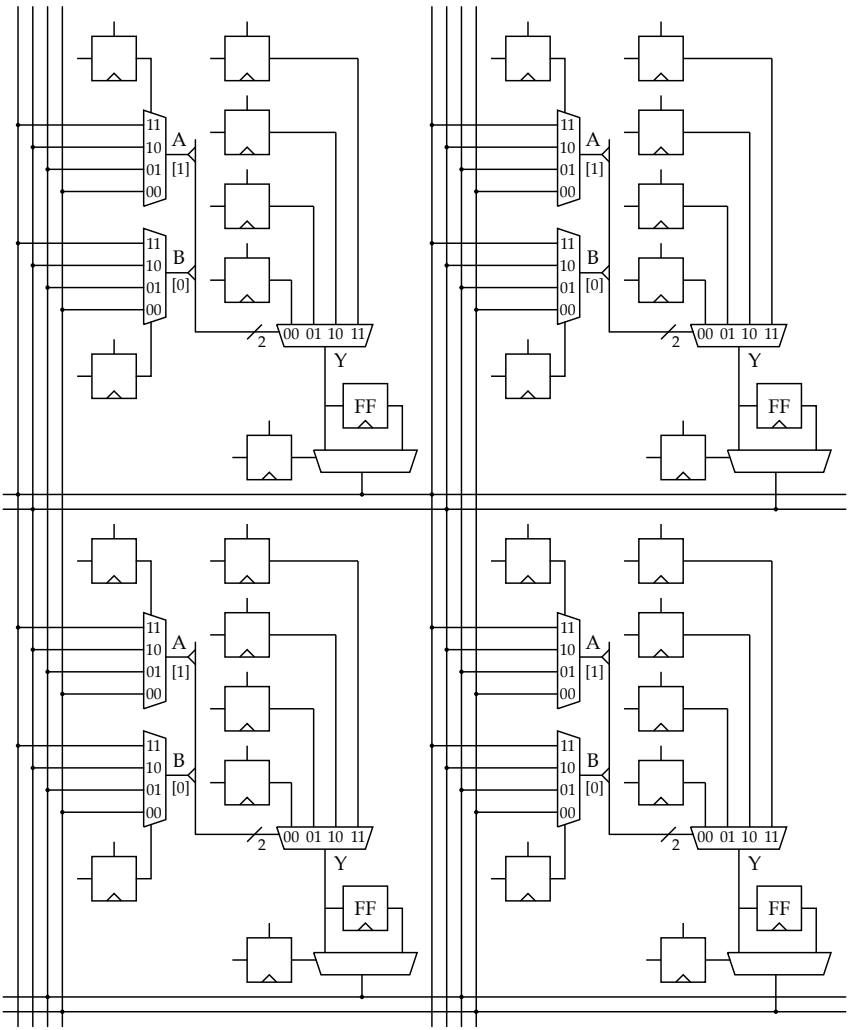
- Programmable logic uses sequential logic-gates to enable reconfiguring ("programming") the behavior of hardware after a chip has been fabricated

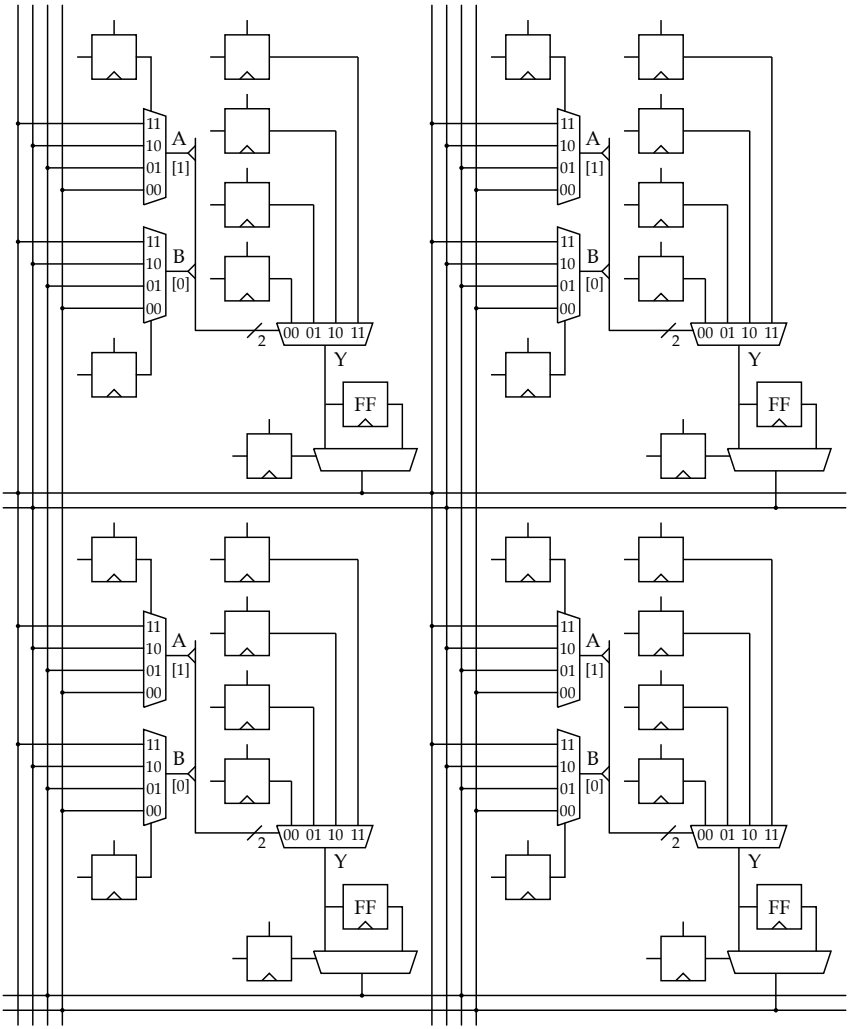
7.1. Programmable Truth Tables

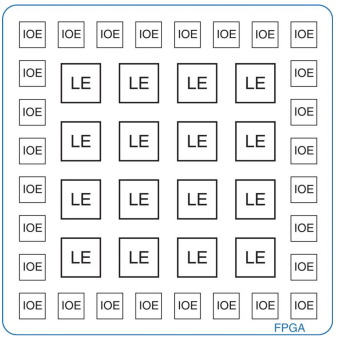


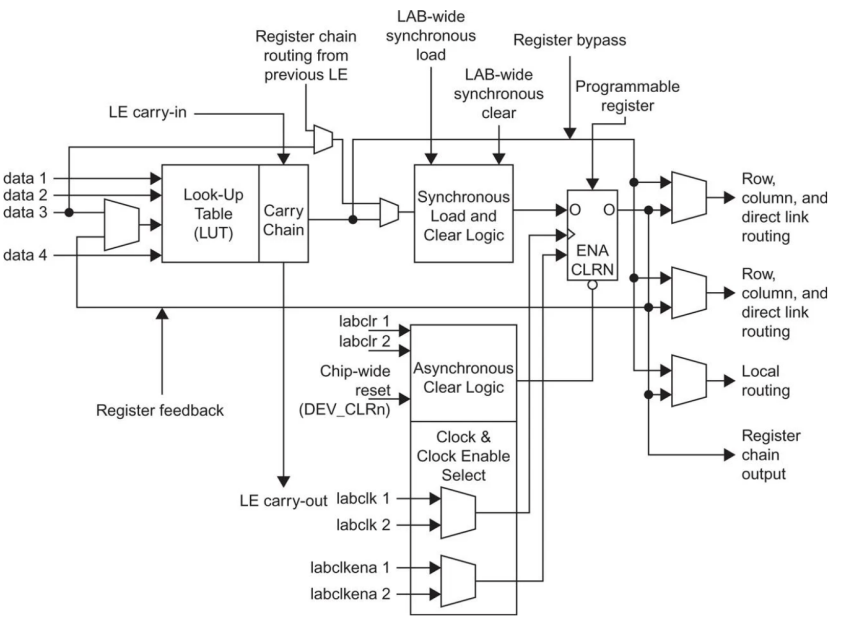

A
[1]
B
[0]
2
00 01 10 11
Y

7.2. Field Programmable Gate Arrays




11
10
01
00
A
[1]
B
[0]
2
00 01 10 11
Y
FF


IOE
LE
FPGA


Register chain routing from previous LE
LAB-wide synchronous load
Register bypass
LAB-wide synchronous clear
Programmable register
LE carry-in
data 1
data 2
data 3
data 4
Look-Up Table (LUT)
Carry Chain
Synchronous Load and Clear Logic
ENA
CLRN
Row, column, and direct link routing
Row, column, and direct link routing
Local routing
Register chain output
labclr 1
labclr 2
Chip-wide reset (DEV_CLRn)
Asynchronous Clear Logic
Clock & Clock Enable Select
Register feedback
LE carry-out
labclk 1
labclk 2
labclkena 1
labclkena 2