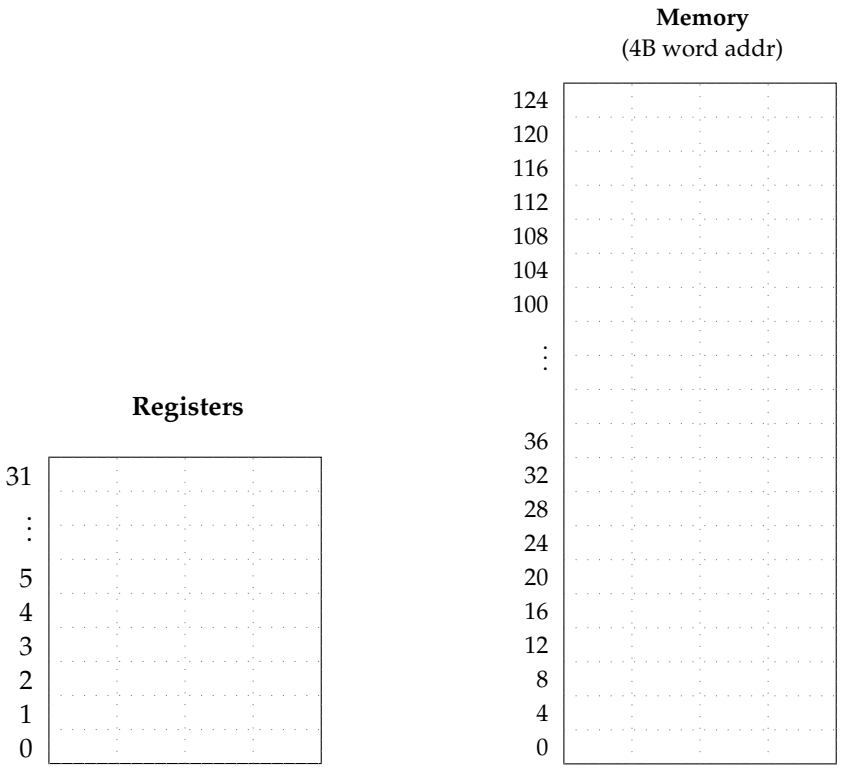
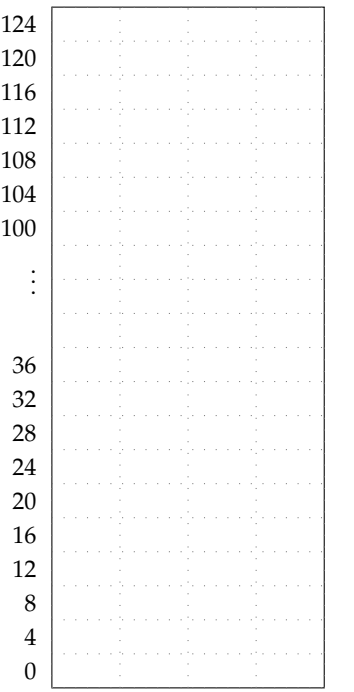
```
01 lw x1, 0(x2)
02 lw x1, 4(x2)
03 sw x1, 0(x2)
04 sw x1, 8(x2)
```

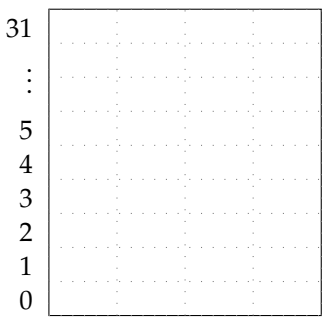


```
01   bne  x1, x0, L1
02   addi x2, x0, 13
03   jal  x0, L2
04 L1:
05   addi x2, x0, 42
06 L2:
```

Memory
(4B word addr)

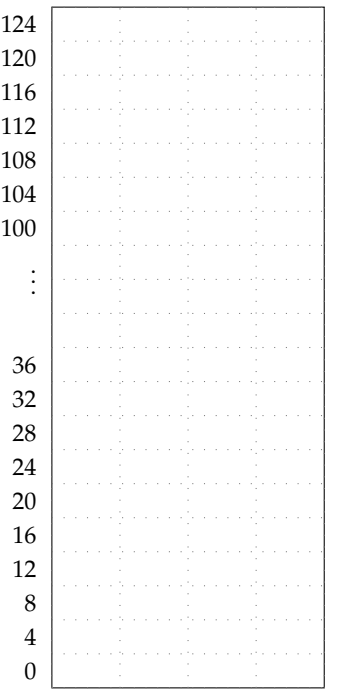


Registers

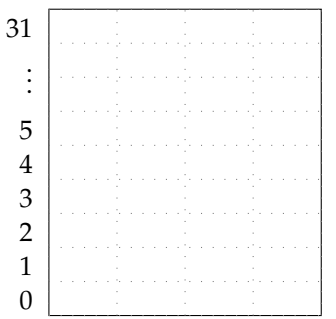


```
01   bne  x1, x0, L1
02   addi x2, x0, 13
03   jal  x0, L2
04 L1:
05   addi x2, x0, 42
06 L2:
```

Memory
(4B word addr)

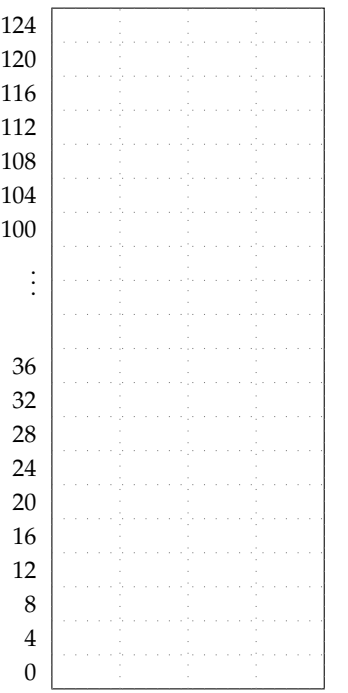


Registers



```
01   addi x1, x0, 0
02 loop:
03   lw   x3, 0(x4)
04   add  x1, x1, x3
05   addi x4, x4, 4
06   addi x2, x2, -1
07   bne  x2, x0, loop
```

Memory
(4B word addr)



Registers