ECE 2300 Digital Logic and Computer Organization, Fall 2025

Discussion Section 2 – Verilog Combinational Gate-Level Design

revision: 2025-09-05-11-57

In this discussion section, we will be implementing a 3-input pair/triple detector as the target hardware in this discussion section. A pair/triple detector has some number of input ports and one output port. The output is one if either two or three of the inputs are one, and the output should be zero otherwise. Here is a truth table and gate-level network for a three-bit pair/triple detector.

in0	in1	in2	out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1