ECE 2300
Digital Logic & Computer Organization

Spring 2025

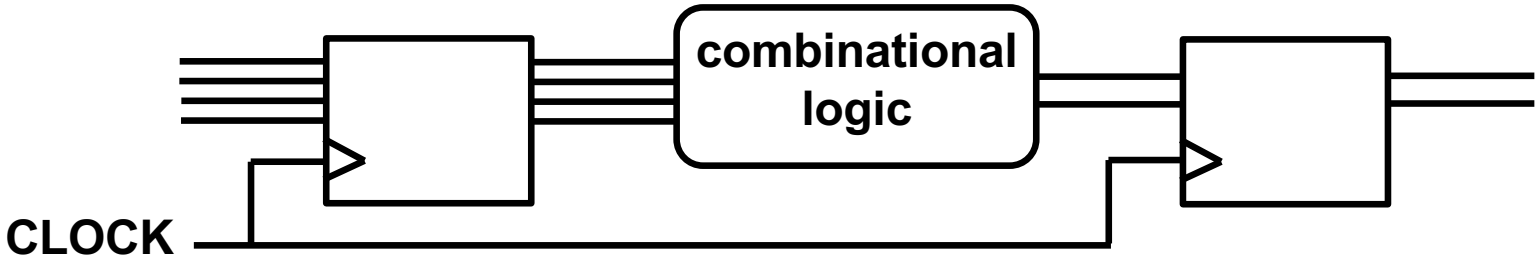
Timing Analysis

Cornell University

Announcements

- **Prelim 1 graded**
  - **Mean: 39.2 (out of 50); Median: 40; High: 50**
- **Lab 3 teaming starts soon; complete it by next Wed to earn a bonus!**
- **Instructor OH today cancelled today**

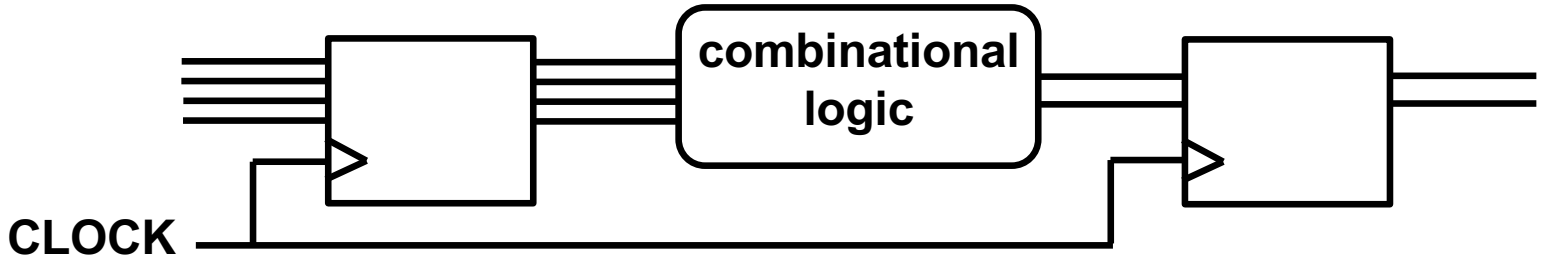
Synchronous Circuits



- The changes in the state of the memory elements are synchronized by a clock signal
  - All flip-flops (FFs) are synchronized to capture the inputs *simultaneously* on the clock tick

- Must ensure the output of the combinational logic has *settled* before the next clock tick

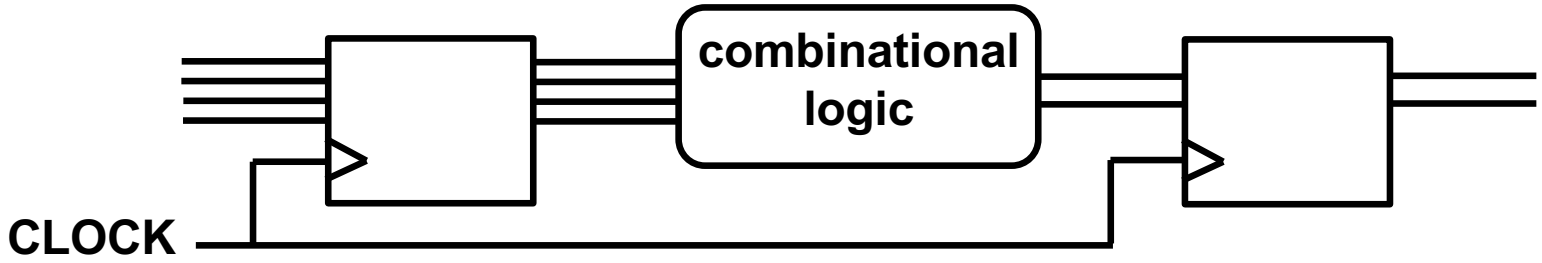
Key Timing Parameters (1)



- Clock cycle time (t_{clk}): also known as the clock period or the clock pulse width
- Combinational logic propagation delay (t_{comb}): the time it takes for a signal to travel through a combinational logic block from input to output.

These are typically design specific

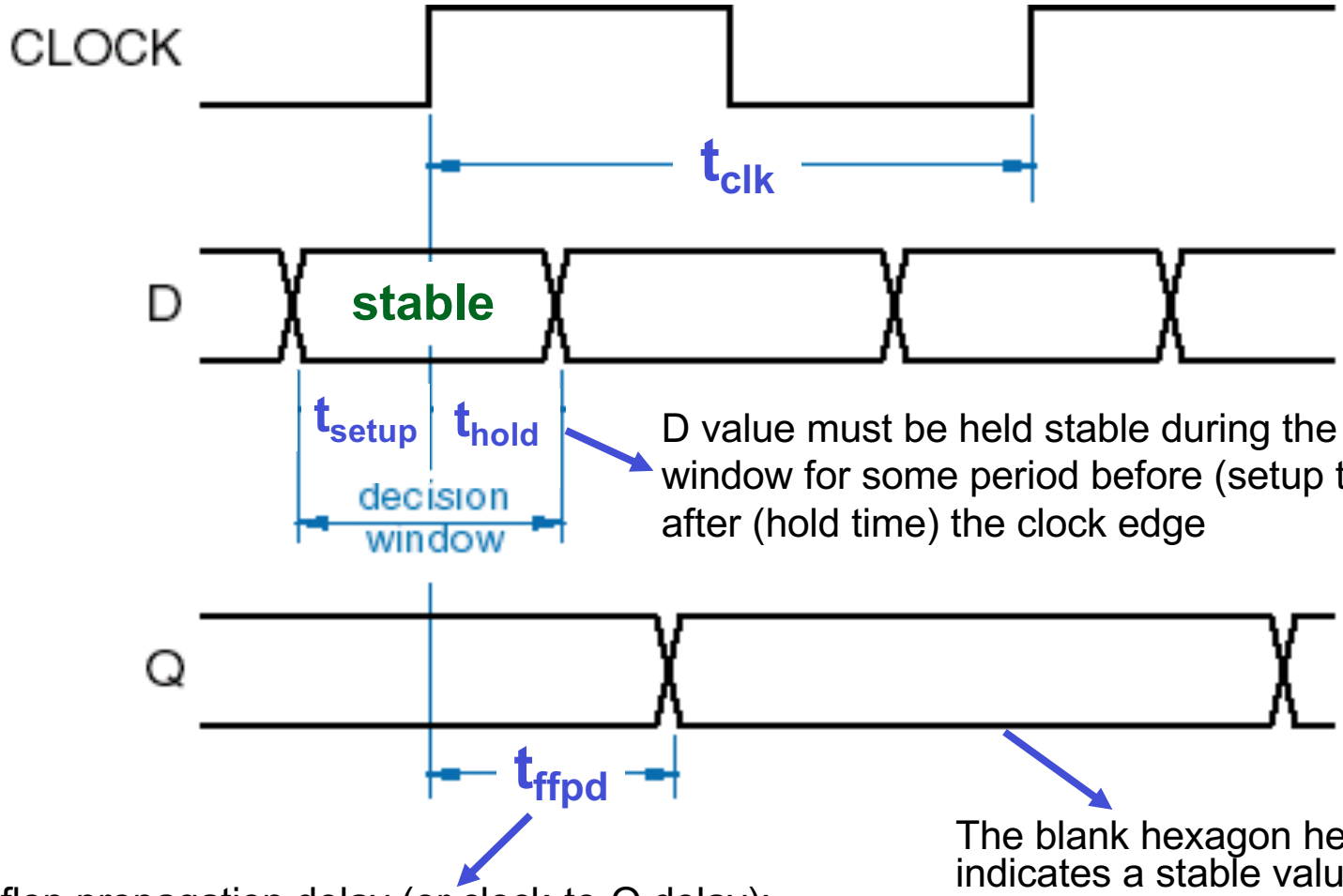
Key Timing Parameters (2)



- Setup time (t_{setup}): The minimum time before the (triggering) clock edge that the data input must be stable
- Hold time (t_{hold}): The minimum time after the clock edge that the data input must remain stable
- Flip-flop propagation delay (t_{ffpd}): the time it takes for the FF output to be stable after the clock edge

The above parameters are typically specified in datasheets by the manufacturer

Stable FF Situation

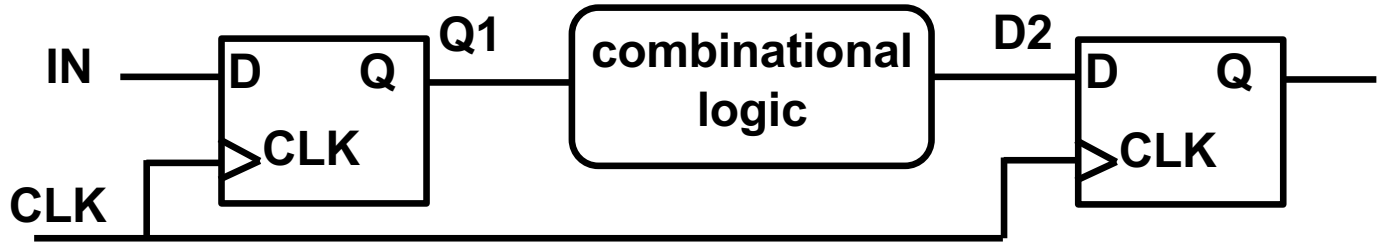


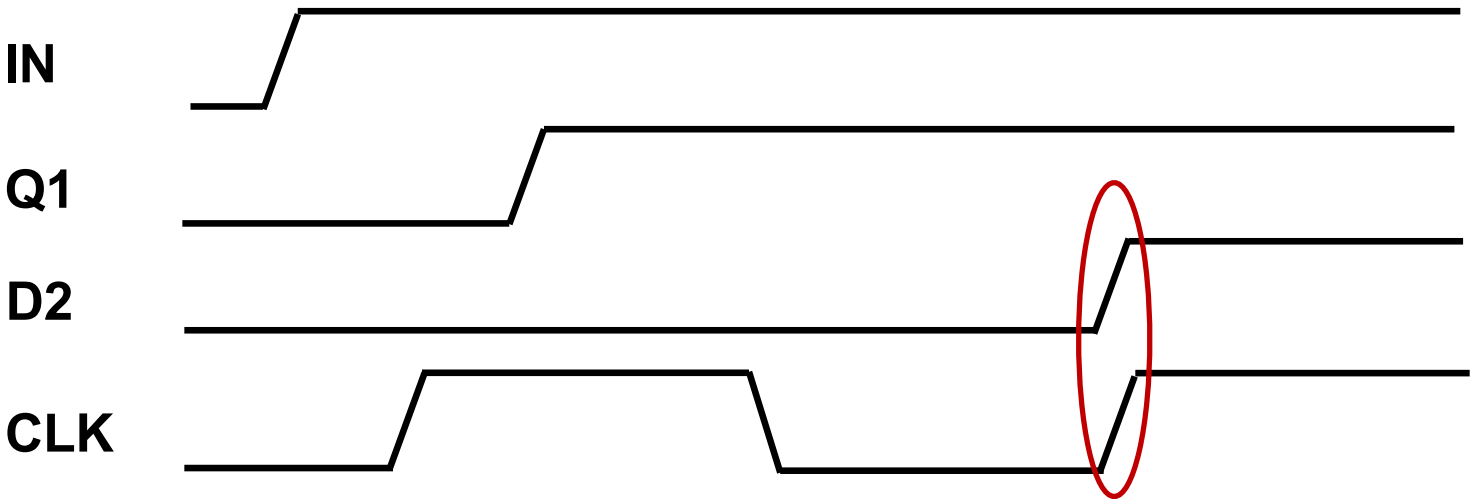
D value must be held stable during the decision window for some period before (setup time) and after (hold time) the clock edge

The blank hexagon here indicates a stable value

Flip-flop propagation delay (or clock-to-Q delay): the time it takes for the FF output to be stable after the clock edge

What if This Happens?

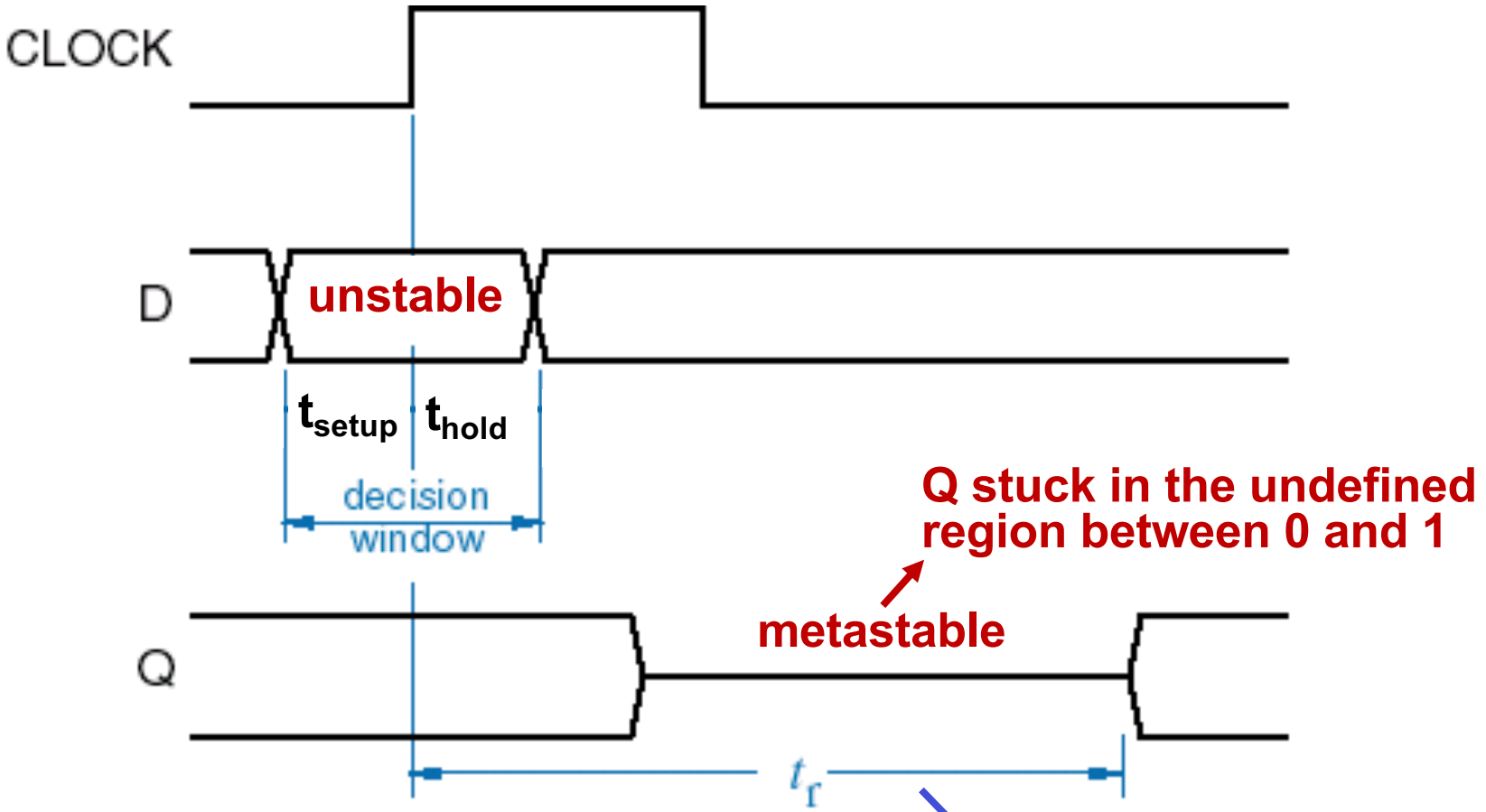




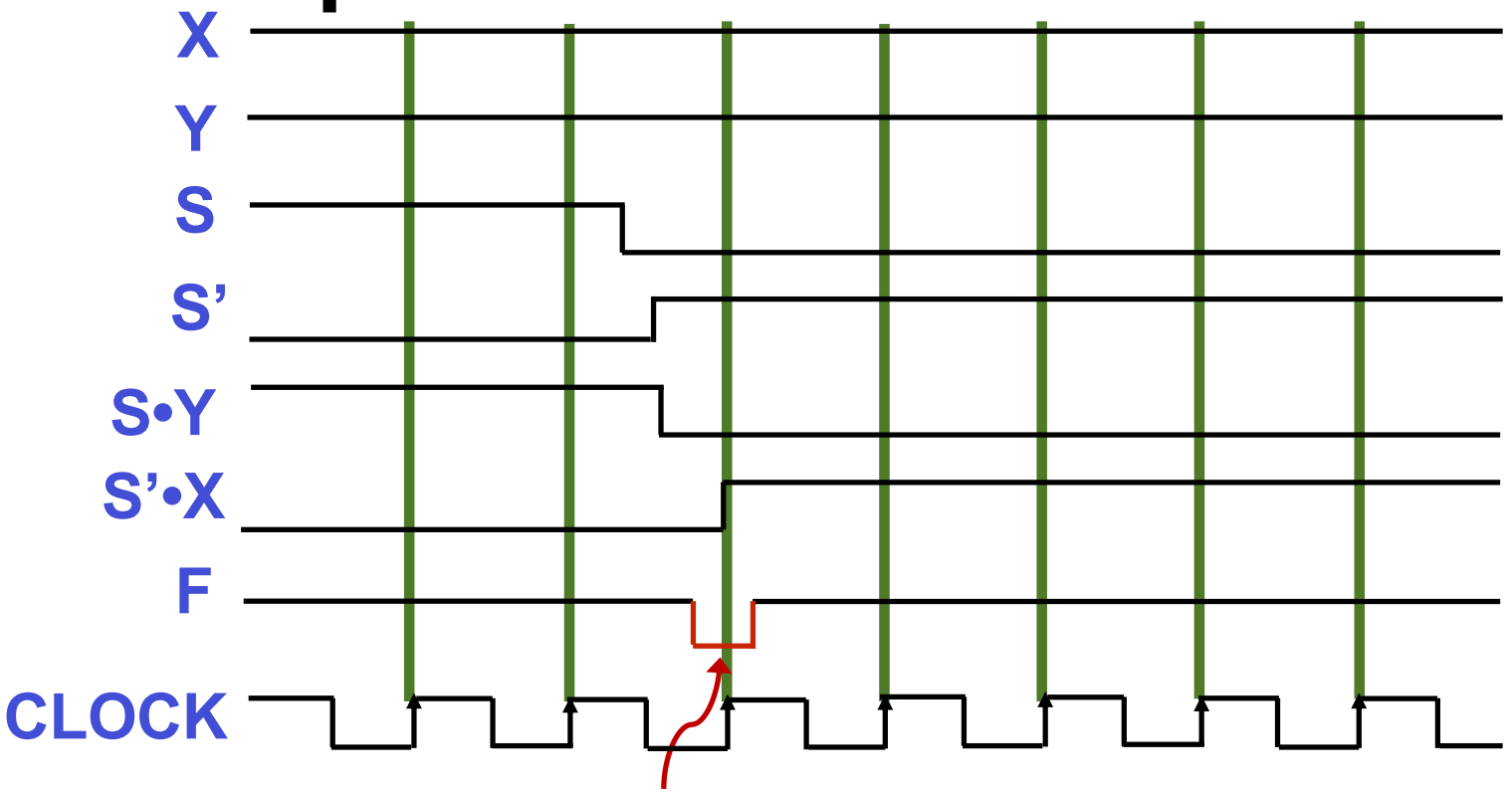
D2 input still transitioning (not stable)

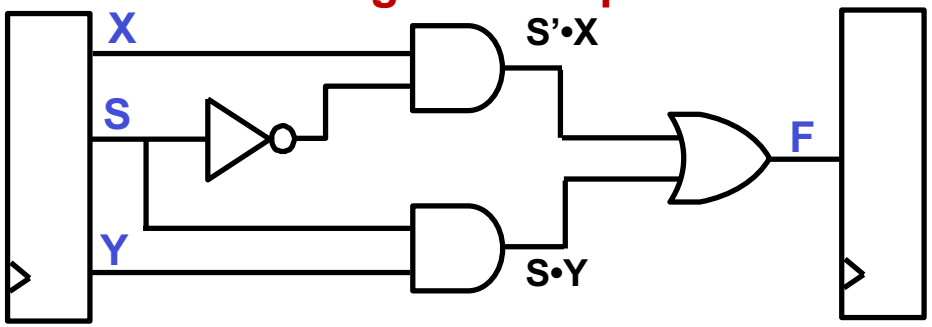
FF may capture neither 0 nor 1

Metastable State



Recap: What About This Situation?





Avoiding Timing Failure

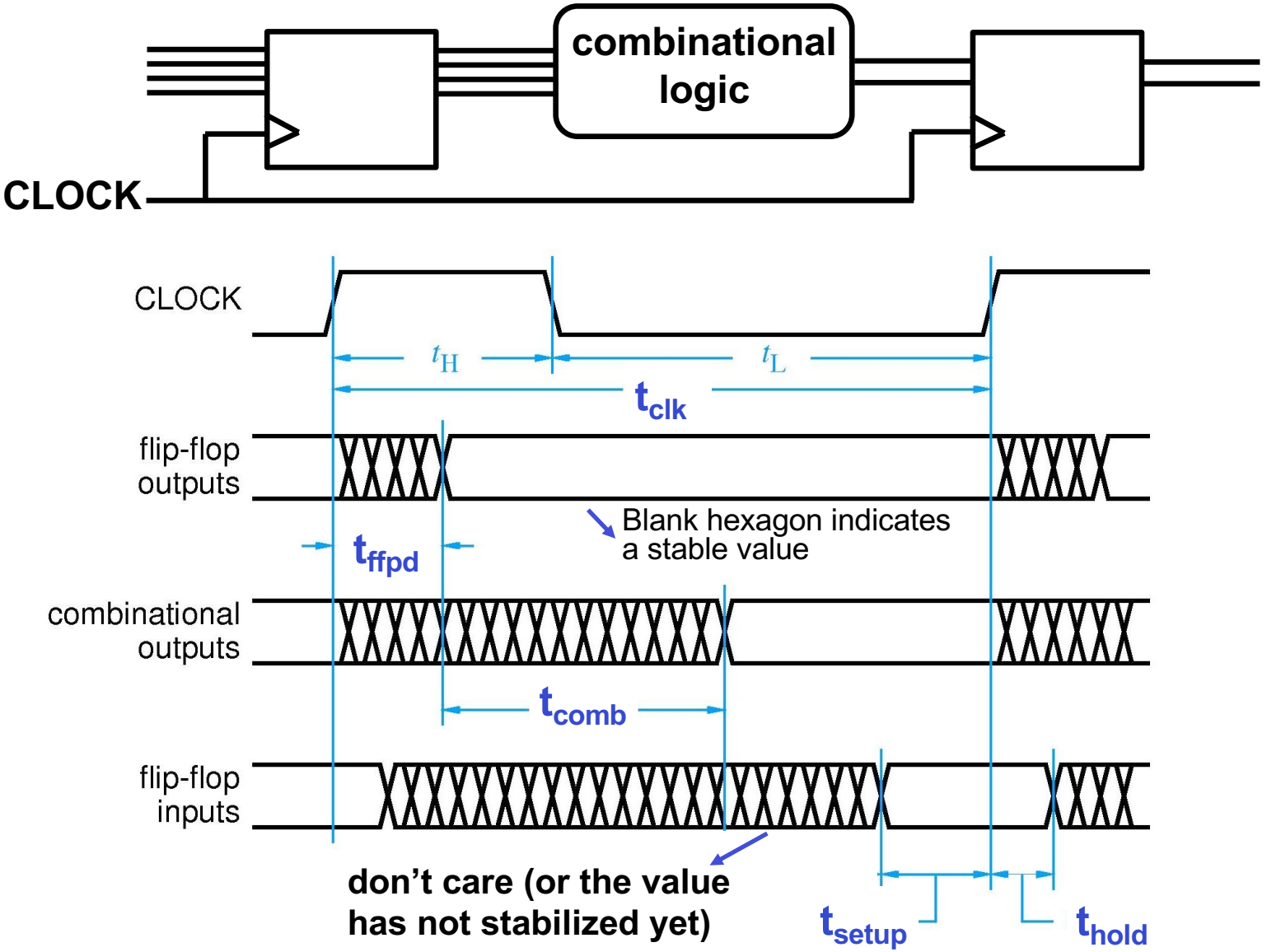
- Possible causes of metastability and wrong value capture
  - Clock pulse that is too narrow
  - Input changes too soon before a clock edge
  - Input changes too soon after a clock edge

- Require timing analysis to ensure the design meets setup time, hold time, and minimum clock pulse width specifications

Sequential Circuit Timing Analysis

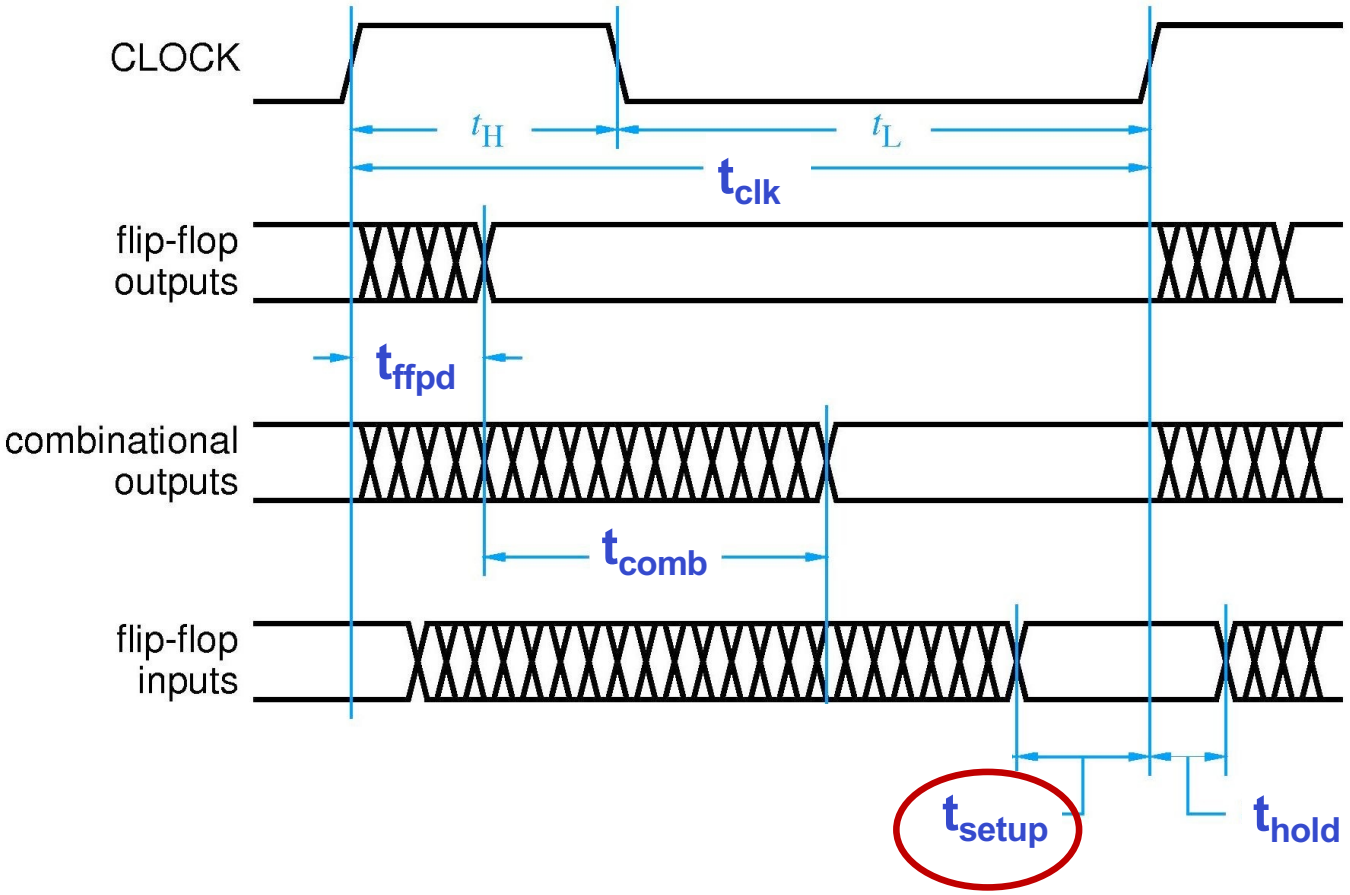
- Timing analysis involves calculating the time delays between all FF pairs within the circuit
- To determine the maximum operating frequency and ensure that setup time requirements are met
  - The clock cannot be too fast
- To ensure that hold time requirements are met
  - The minimum propagation delay of the combinational logic (contamination delay) cannot be too small
  - Independent of clock cycle time

Important Timing Parameters

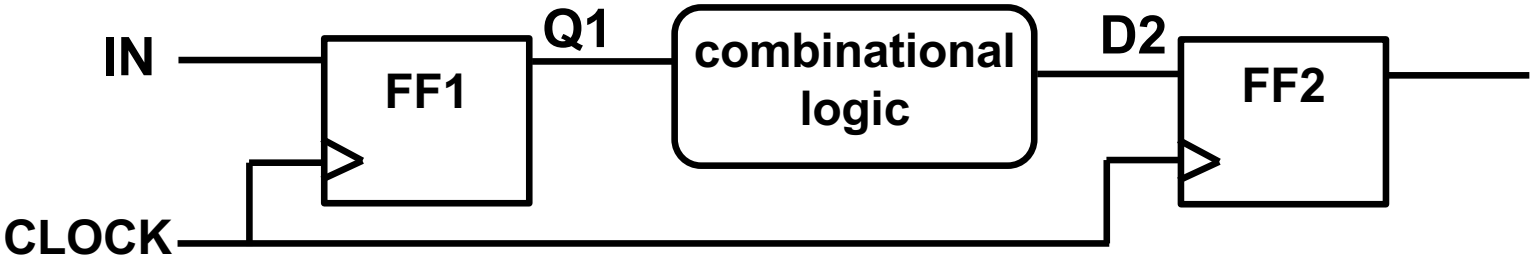


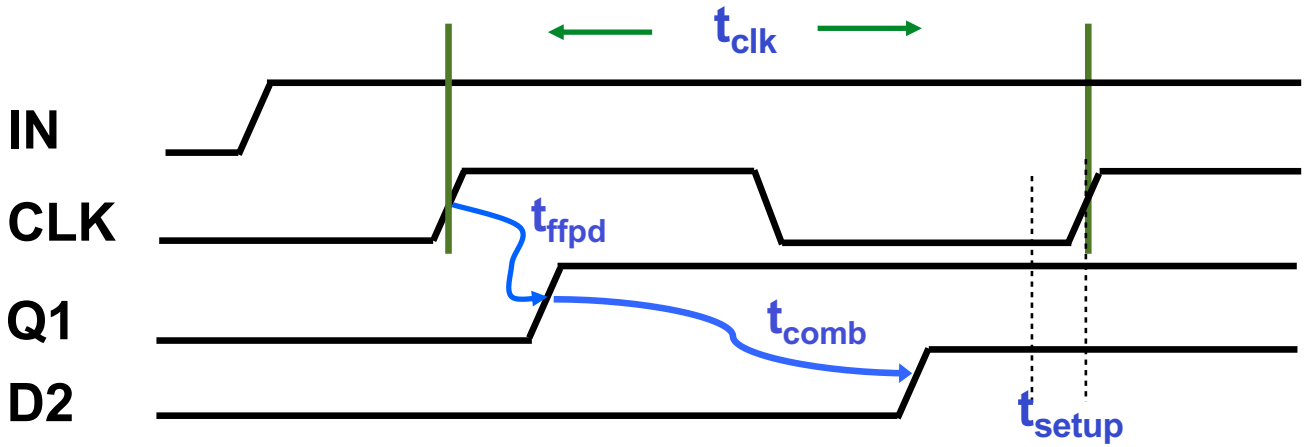
Setup Time Constraint

- t_{setup} is the minimum amount of time before the triggering edge during which FF input must be stable



Meeting Setup Time Constraint



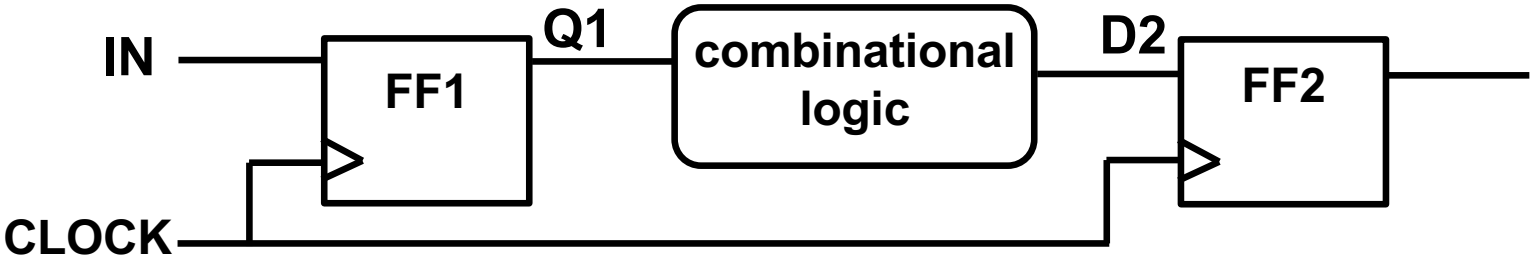


D2 must stabilize <u>before</u> the t_{setup} window

$$t_{clk} - t_{setup} \geq t_{ffpd(max)} + t_{comb(max)}$$

We use the maximum delay here because it represents the worst-case scenario for meeting setup time. If the maximum propagation delay satisfies the inequality, the minimum delay case automatically holds, since $t_{ffpd(max)} + t_{comb(max)} \geq t_{ffpd(min)} + t_{comb(min)}$

Determining Clock Cycle Time

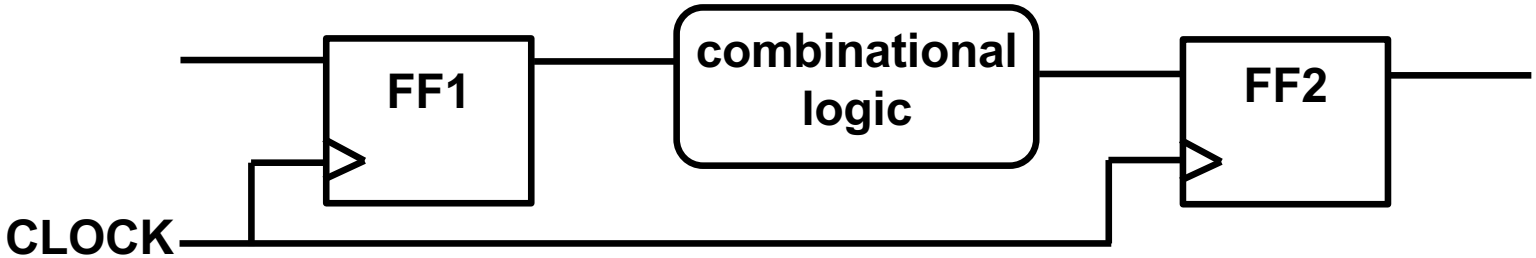


- $t_{clk} \geq t_{ffpd(max)} + t_{comb(max)} + t_{setup}$

  Every circuit path between every pair of FFs must satisfy the above equation to run the circuit at a frequency of $1/t_{clk}$

- **Consider maximum propagation delays (the longest timing path) to determine the maximum clock frequency**
  - **Worst case temperature and voltage**
  - **Worst case manufacturing variations**

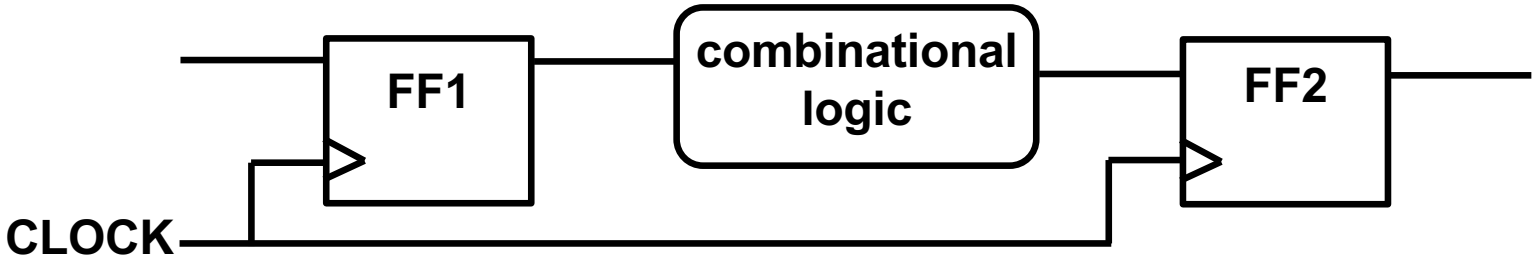
Example: Cycle Time Calculation



	Prop Delay (ns)		Setup Time (ns)	Hold Time (ns)
	min	max		
FF	1	2	3	1
Comb	3	7	-	-

What's the best achievable cycle time?

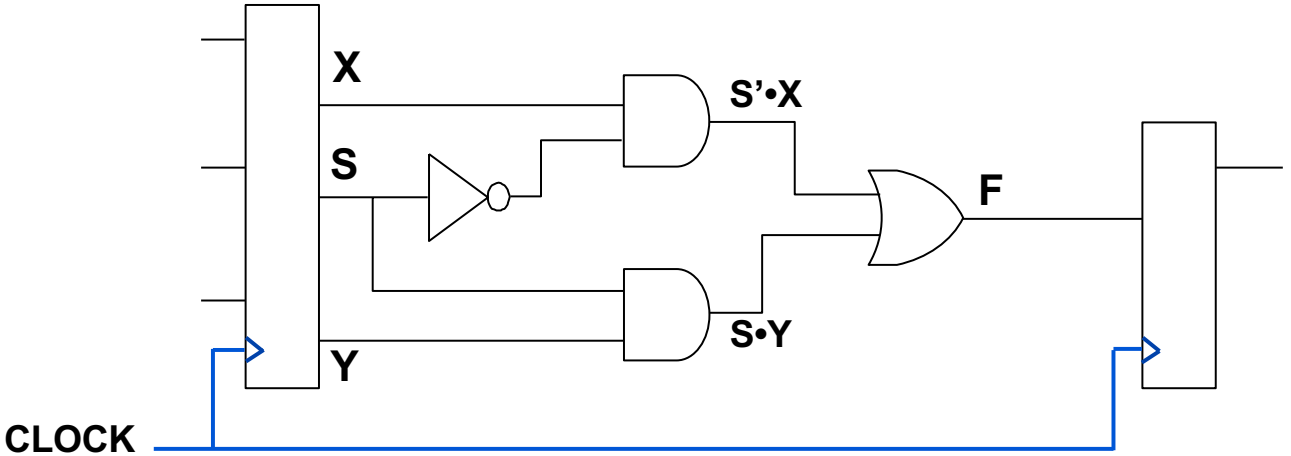
Example: Cycle Time Calculation



	Prop Delay (ns)		Setup Time (ns)	Hold Time (ns)
	min	max		
FF	1	2	3	1
Comb	3	7	-	-

$$t_{clk} \geq t_{ffpd(max)} + t_{comb(max)} + t_{setup} = 2 + 7 + 3 = 12ns$$

Exercise: Cycle Time Analysis

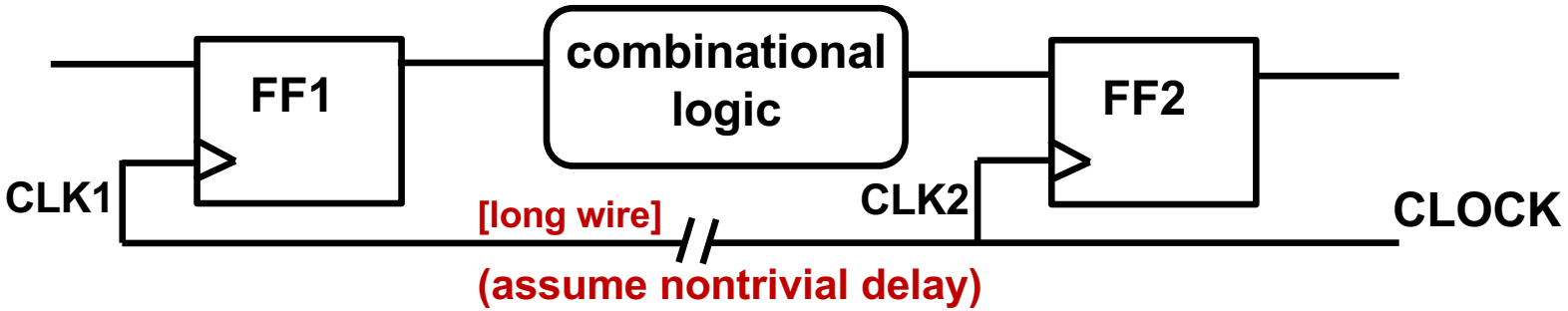


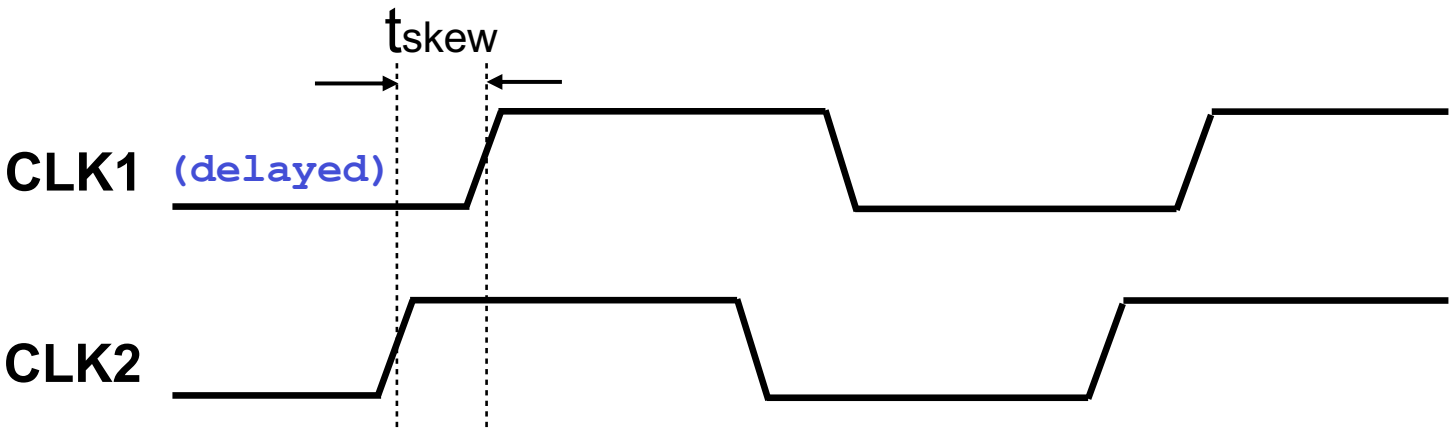
Assumptions:
(1) FF propagation delay = 1ns
(2) Uniform gate delay = 1ns
(3) Setup time = 2ns, hold time = 2ns

What's the best achievable cycle time?

Clock Skew Complicates Matters Further

- Clock may not reach all flip-flops simultaneously

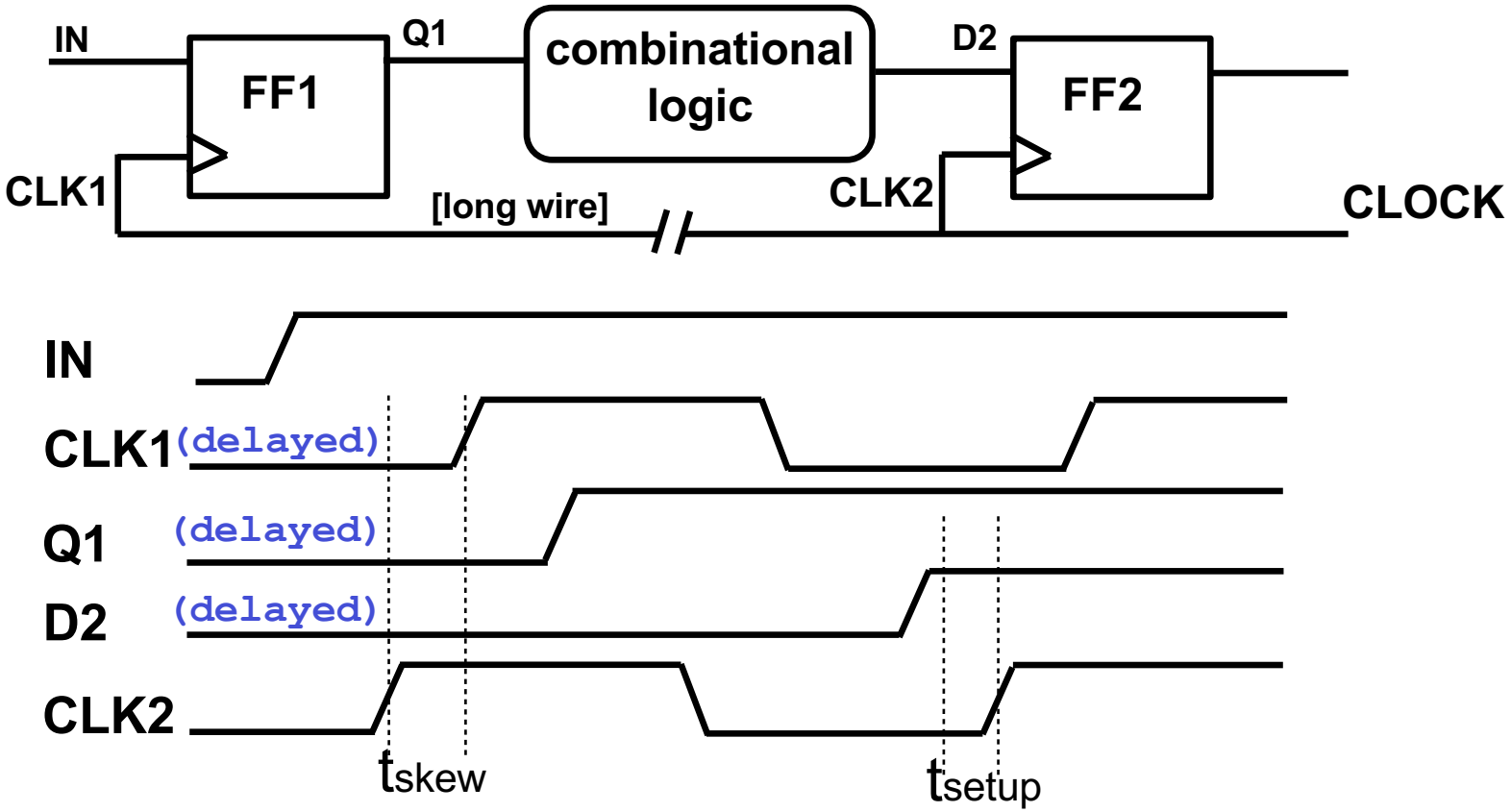




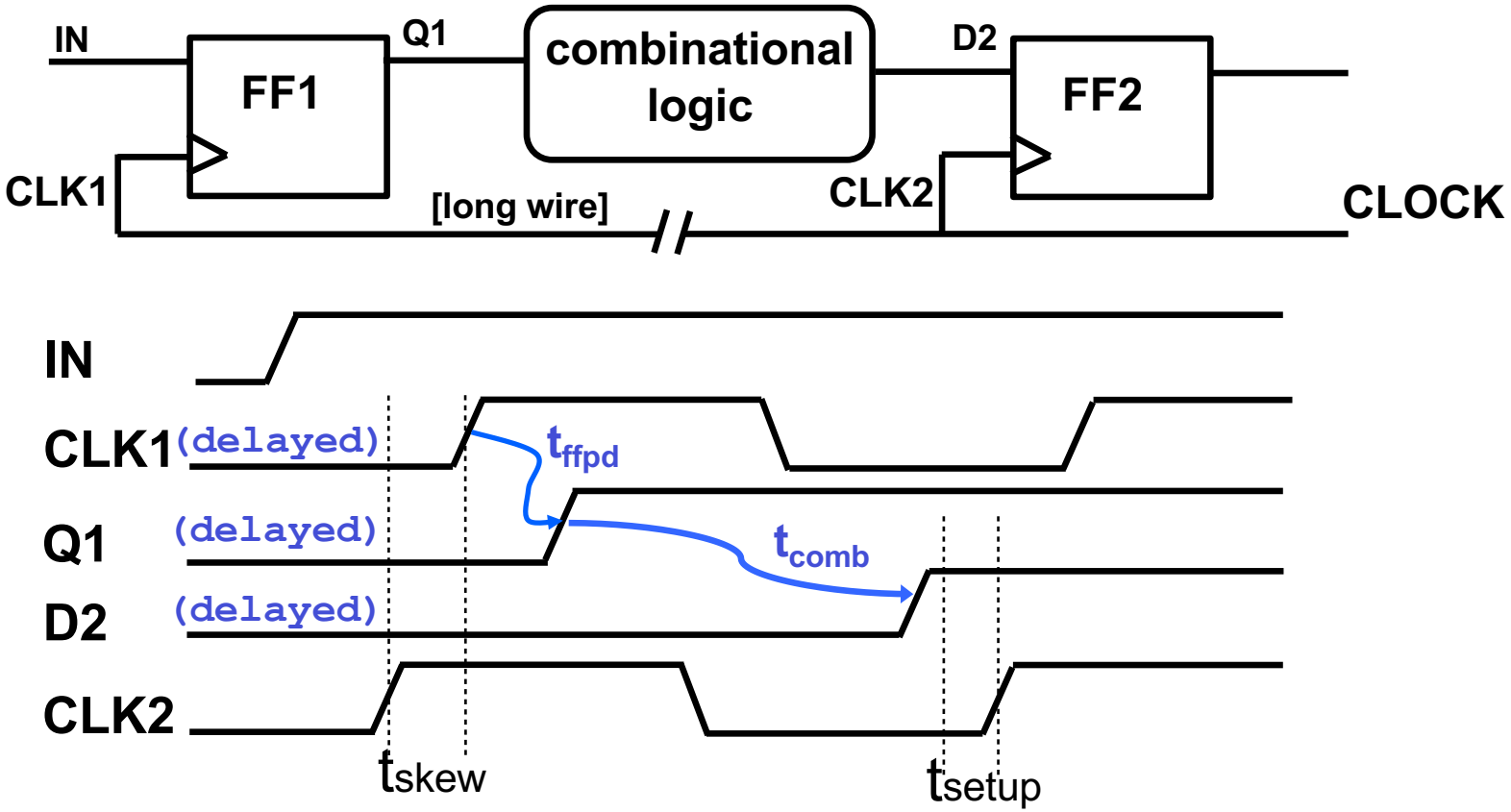
$t_{skew(max)}$: Maximum clock skew

$t_{skew(min)}$: Minimum clock skew

Setup Time Analysis With Clock Skew



Negative Clock Skew

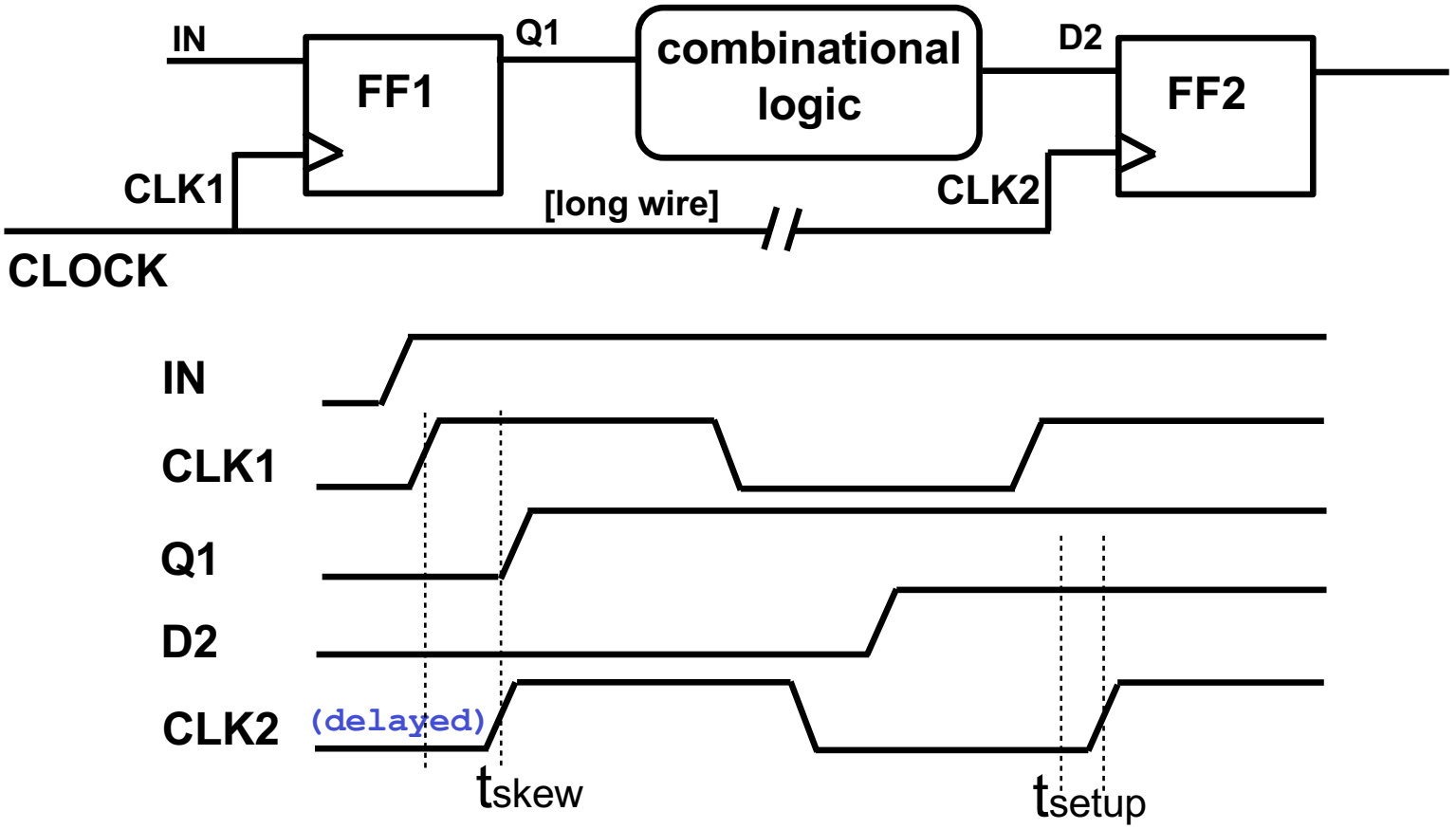


Sending FF receives clock later than receiving FF

$$t_{ffpd(max)} + t_{comb(max)} + t_{setup} \leq t_{clk} - t_{skew(max)}$$

Harmful skew for meeting setup time constraint

Positive Clock Skew

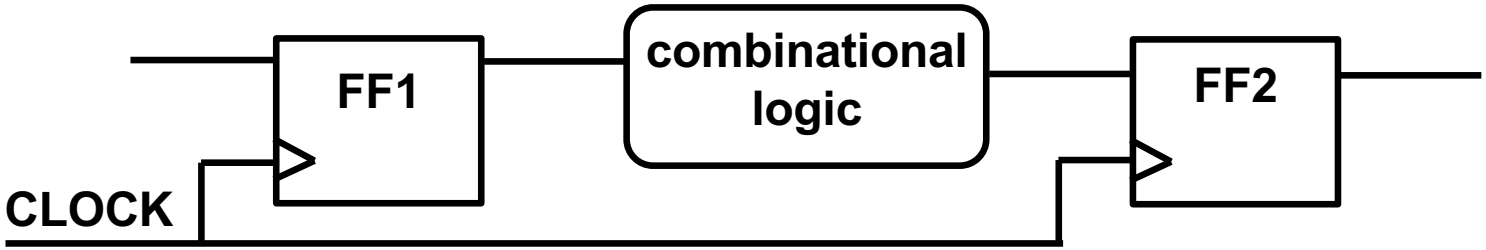


Sending FF receives clock sooner than receiving FF

$$t_{ffpd(max)} + t_{comb(max)} + t_{setup} \leq t_{clk} + t_{skew(min)}$$

Beneficial skew for meeting setup time constraint

Example: Setup Analysis with Clock Skew

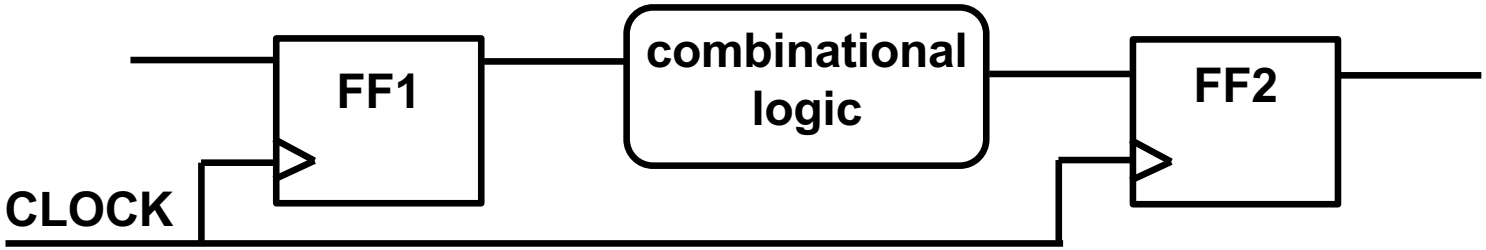


Clock arrives at FF1 at least 4ns earlier than FF2

	Prop Delay (ns)		Setup Time (ns)	Hold Time (ns)
	min	max		
FF	1	2	3	1
Comb	3	7	-	-

- What's the best achievable cycle time?

Example: Setup Analysis with Clock Skew



Clock arrives at FF1 at least 4ns earlier than FF2

	Prop Delay (ns)		Setup Time (ns)	Hold Time (ns)
	min	max		
FF	1	2	3	1
Comb	3	7	-	-

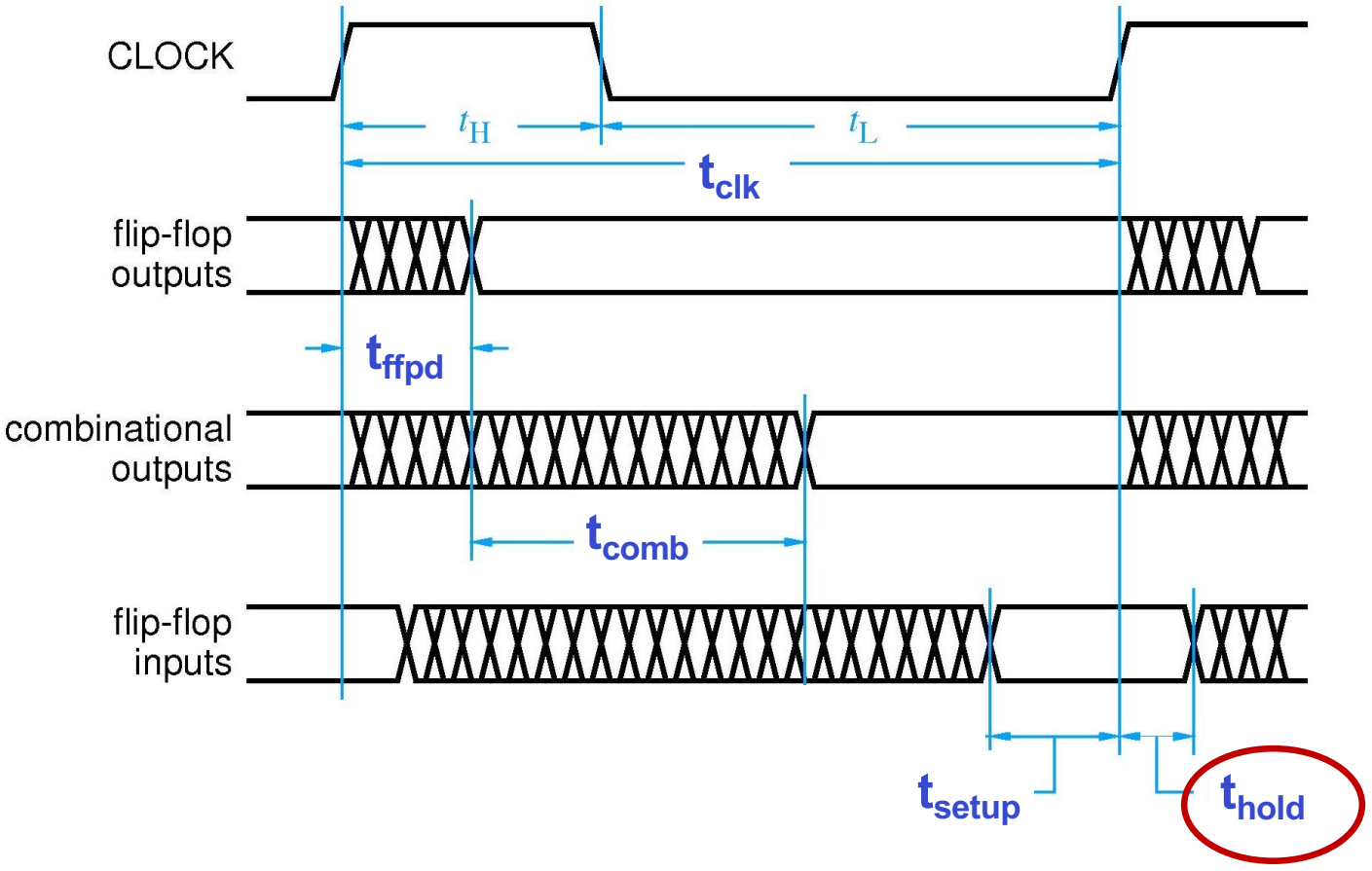
- What's the best achievable cycle time?

$t_{ffpd(max)} + t_{comb(max)} + t_{setup} <= t_{clk} + t_{skew(min)}$

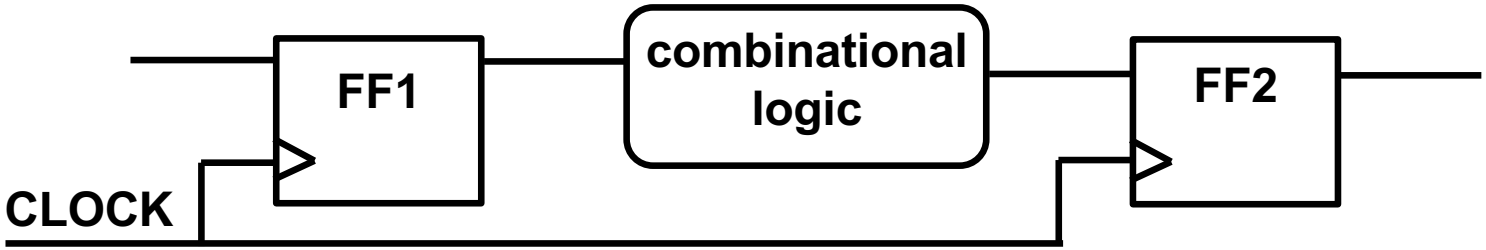
$t_{clk} >= 2 + 7 + 3 - 4 = 8ns$

Hold Time Constraint

- **t_{hold} is the minimum amount of time after the triggering edge during which *FF input must remain stable***



Avoiding Hold Time Violation



- **FF input must remain stable after the triggering edge by at least t_{hold} amount of time**
  - **Otherwise, the receiving flip-flop may be contaminated with an unexpected value**

- **Need to consider minimum propagation delays (the shortest timing path) for hold time calculations**

$$t_{ffpd(min)} + t_{comb(min)} \geq t_{hold}$$

We'll discuss this next lecture

Next Class

More Timing Analysis
Binary Arithmetic
(H&H 1.4)