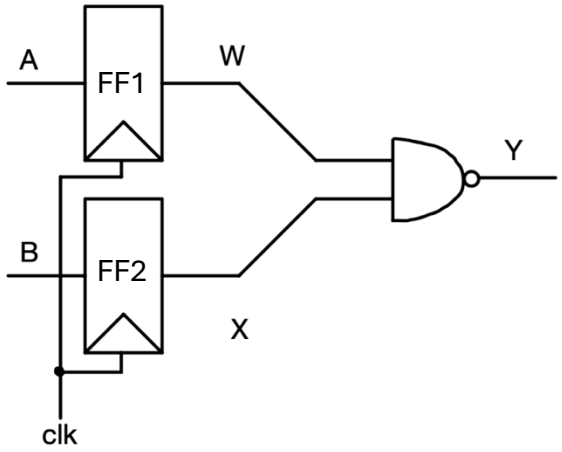
Sequential Logic

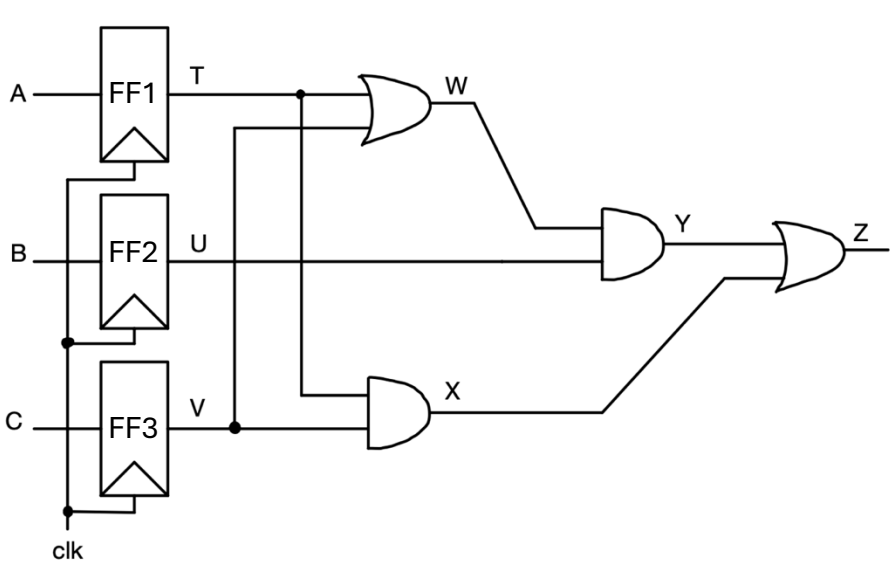
For the following problems complete the simulation table. Assume zero delay model.

1.



clk	A	B	W	X	Y
0	0	0			
1	1	0			
0	1	1			
1	0	1			
0	0	0			
1	1	1			

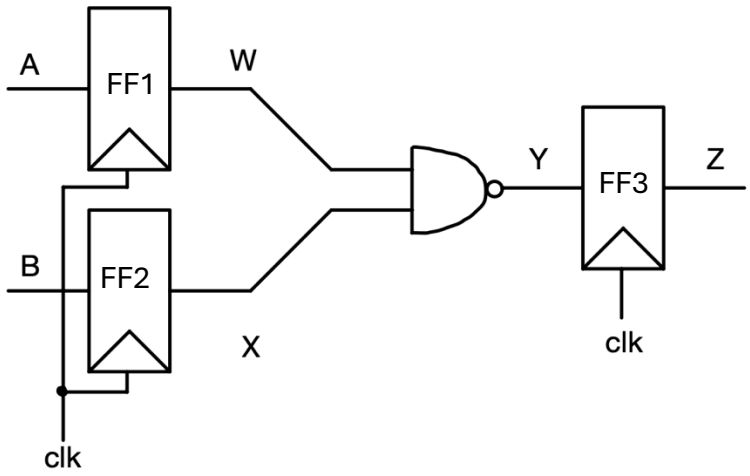
2.



clk	A	B	C	T	U	V	W	X	Y	Z
0	0	0	0							
1	1	0	0							
0	1	1	0							
1	0	1	1							
0	0	1	0							
1	1	1	1							
0	1	0	1							
1	1	1	0							
0	1	0	1							
1	0	0	1							

For the following problems, you will be asked to analyze a sequential gate-level network. Each problem you will be asked to write down all the paths, label the short and critical path(s), compute the minimum clock period given the delay model that is provided, as well as compute hold time constraint using the delay model that is provided. Use $\overline{D_f}$ only for the waveform diagrams.

3.



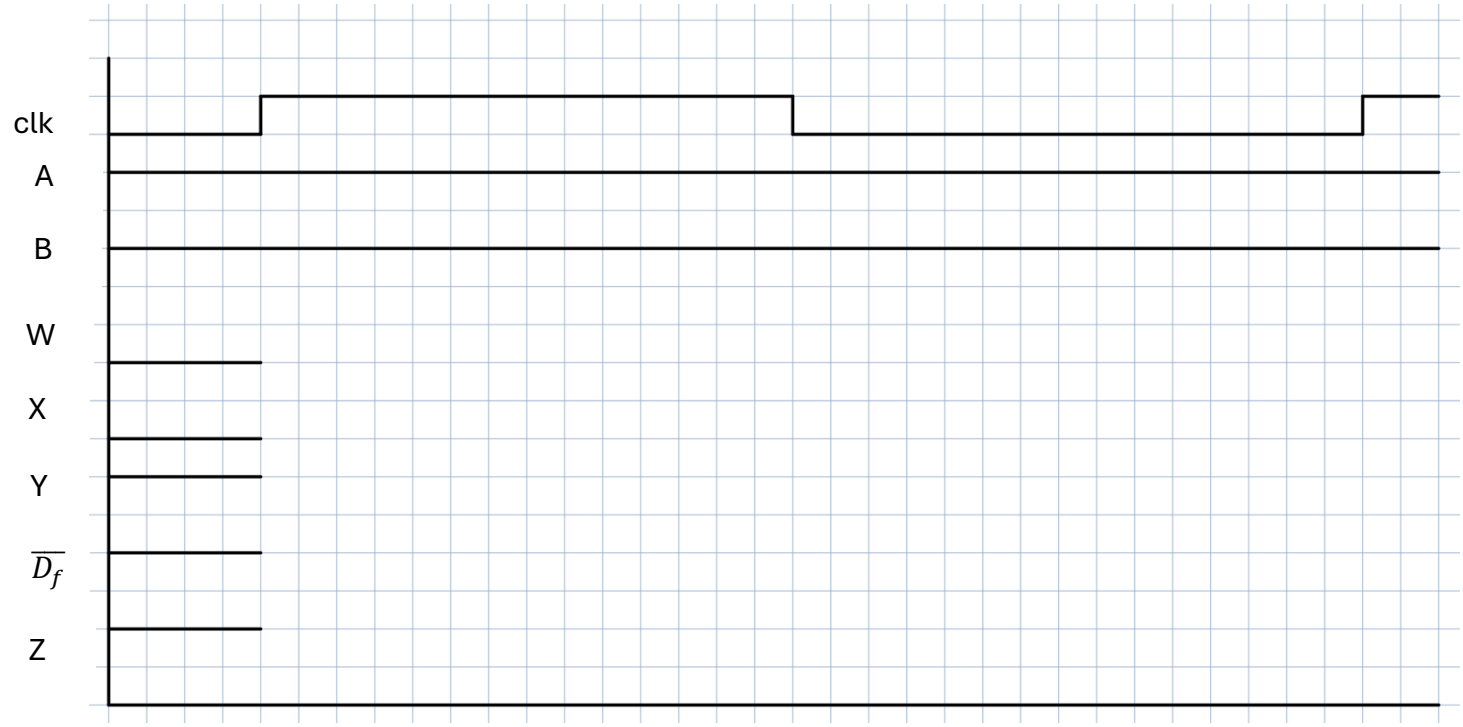
Gate	t_{pd}	t_{cd}
NAND2	2τ	1τ
1-bit FF Clock-to-Q	9τ	-
1-bit FF Setup	10τ	-
Input Clock-to-Port	0τ	-
Output Port Setup	0τ	-

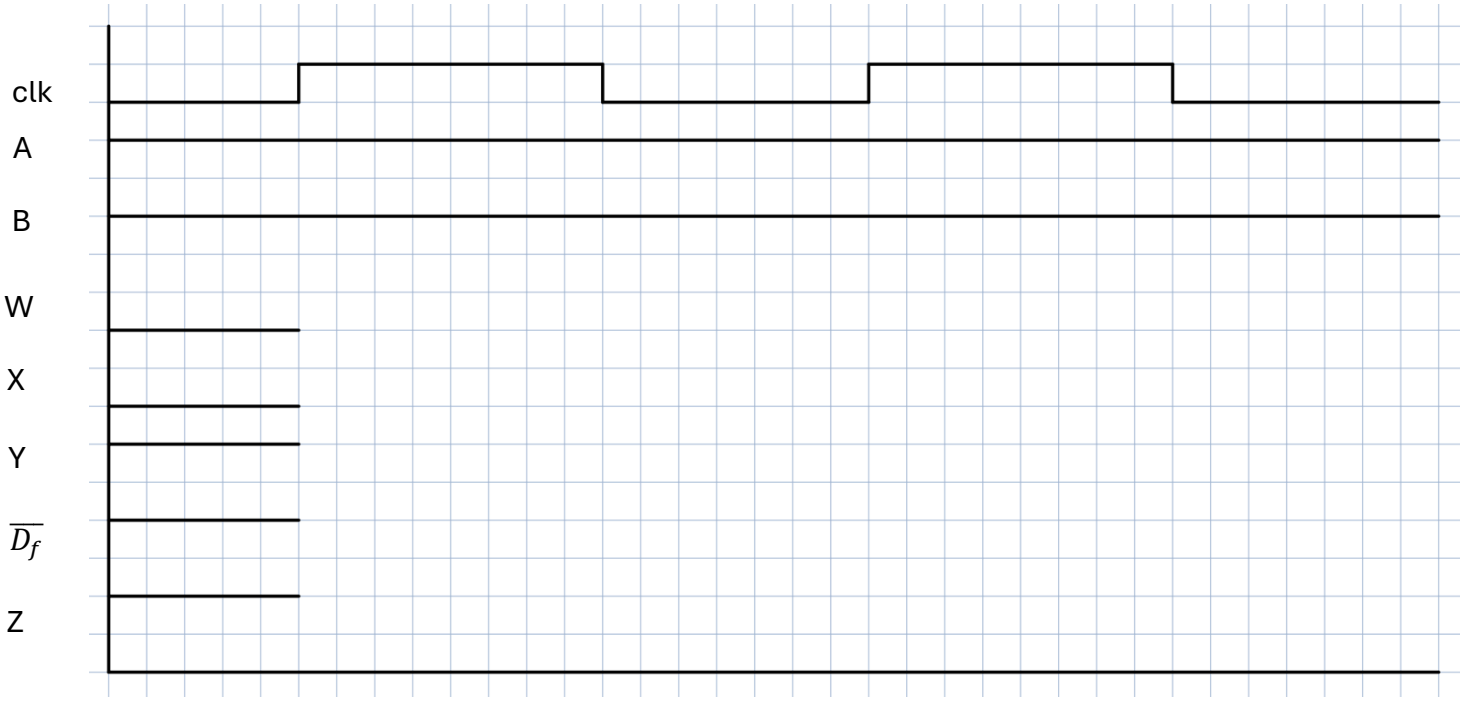
Path	Delay of Each Component on Path	$t_{pd,total}$	$t_{cd,total}$	Critical Path?	Short Path?

a. Compute the hold time, t_{hold}.

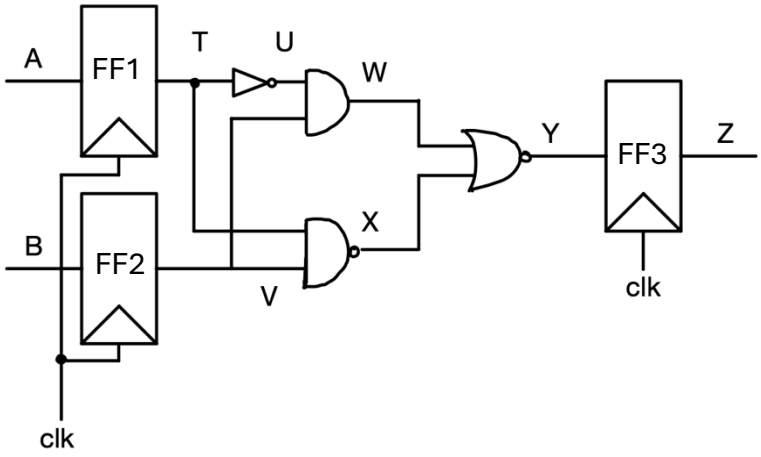
b. What is the minimum clock period T_c in units of τ?

c.





4.

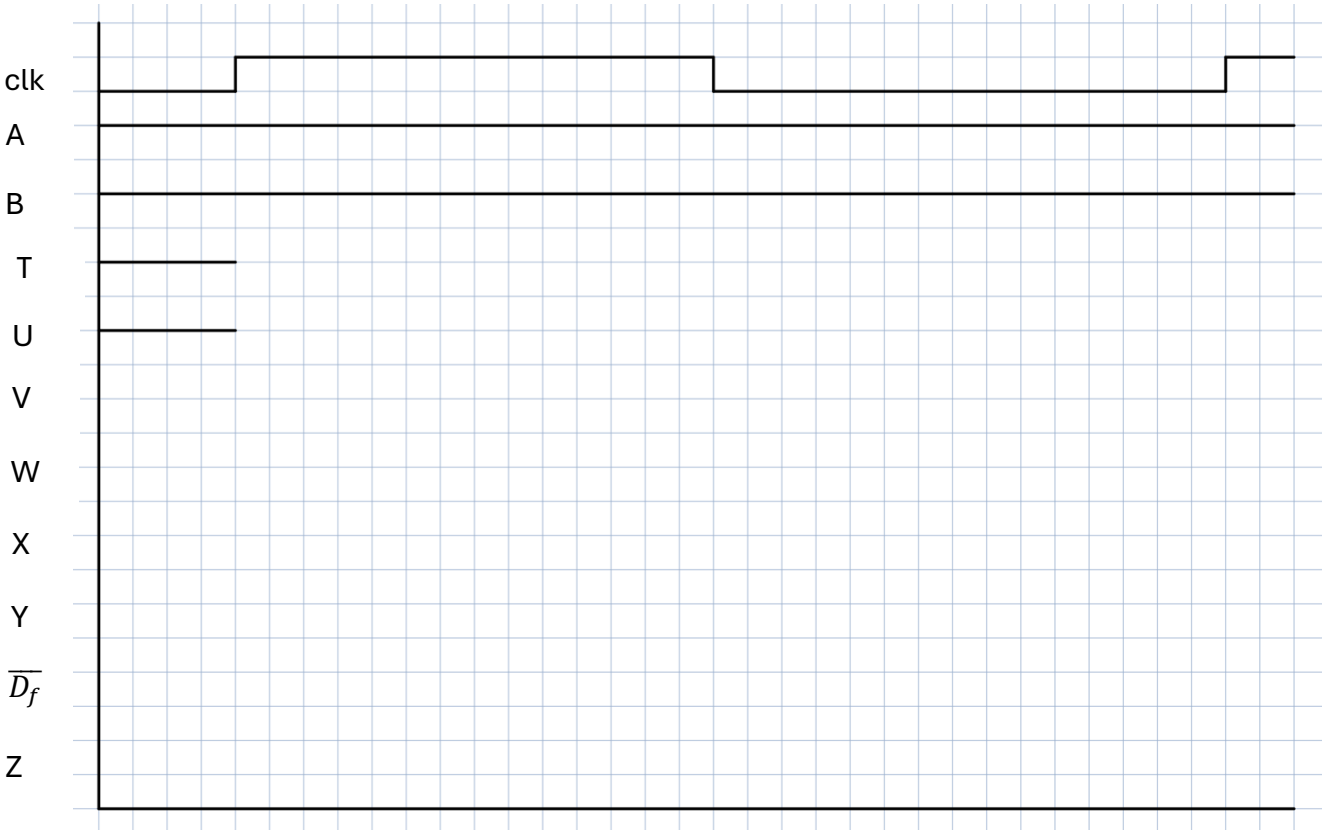


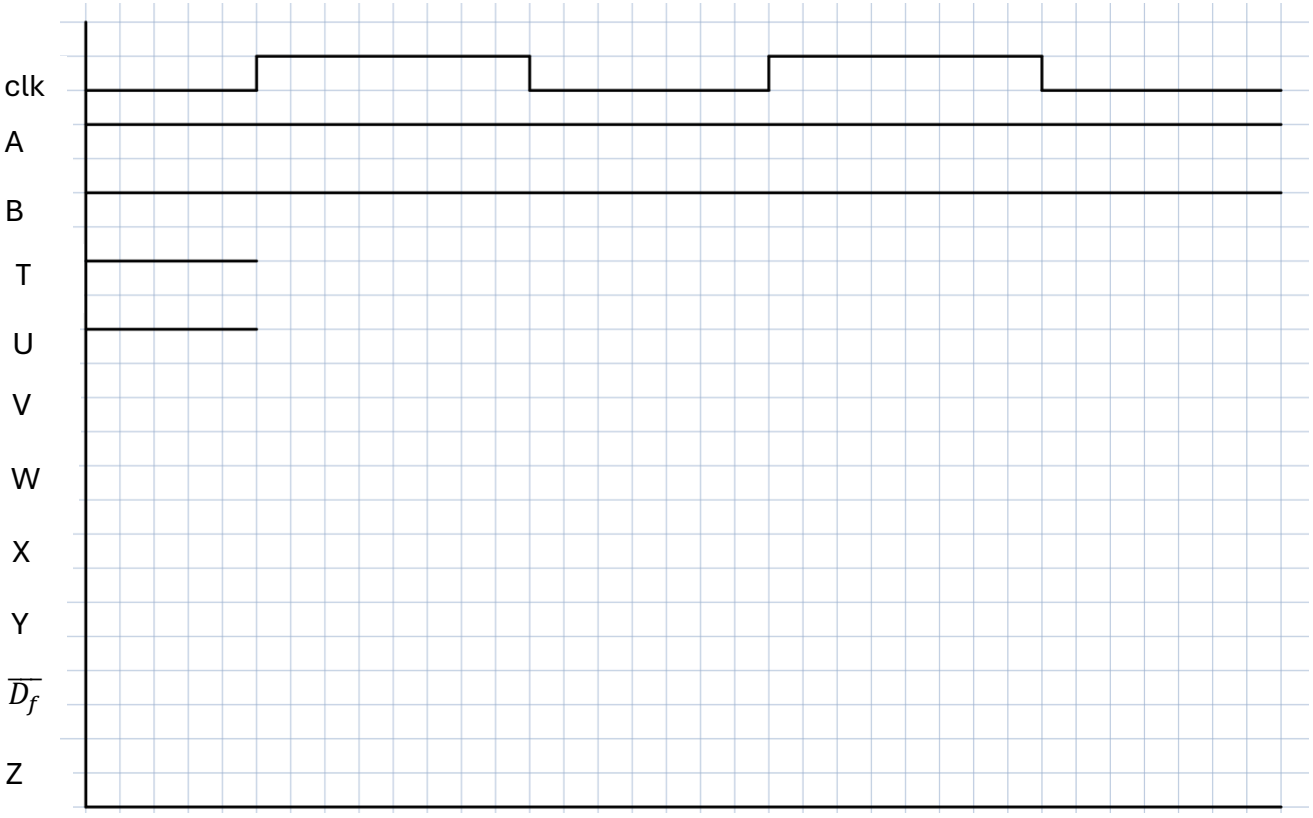
Gate	t_{pd}	t_{cd}
OR2	4τ	1τ
AND2	3τ	1τ
1-bit FF Clock-to-Q	9τ	-
1-bit FF Setup	10τ	-
Input Clock-to-Port	0τ	-
Output Port Setup	0τ	-

Path	Delay of Each Component on Path	$t_{pd,total}$	$t_{cd,total}$	Critical Path?	Short Path?

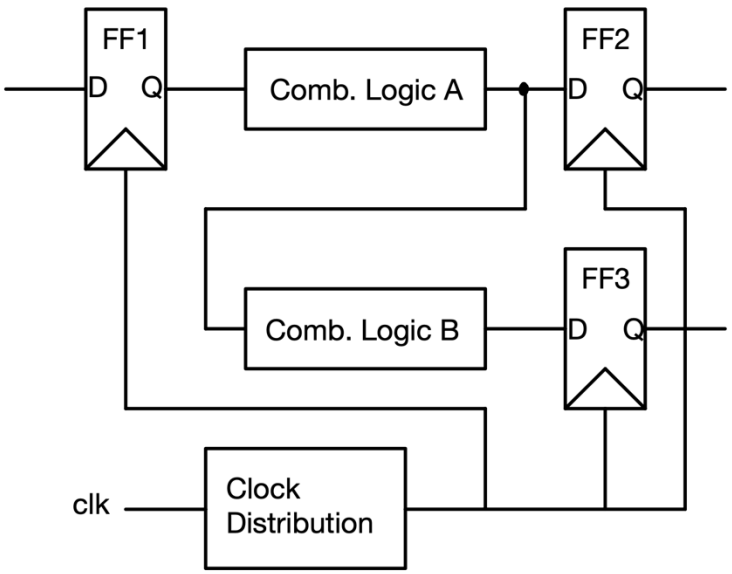
a. Compute the hold time, t_{hold}.
b. What is the minimum clock period T_c in units of τ?

c.




clk
A
B
T
U
V
W
X
Y
$\overline{D_f}$
Z

5.



Component	t_{pd}	t_{cd}	Setup Time	Hold Time	Min Clock Distribution Delay	Max Clock Distribution Delay
FF1	1	4	2	1	2	3
FF2	4	6	2	0	3	5
FF3	2	3	4	2	1	2
Comb Logic A	1	4	-	-	-	-
Comb Logic B	4	6	-	-	-	-

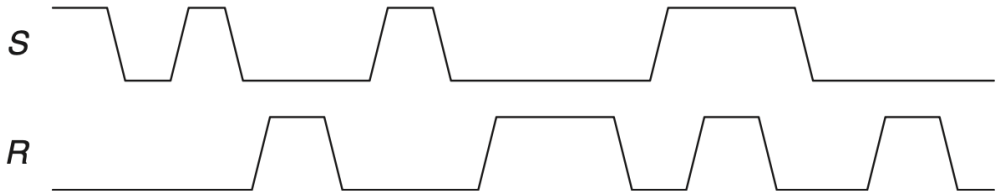
a. Calculate the worst-case clock skew between FF1 and FF2, and between FF1 and FF3, when considering FF2 and FF3 setup time.

b. Determine the fastest cycle time at which the circuit can operate. Justify your answer by analyzing all possible paths in your answer.

c. Calculate the worst-case clock skew between FF1 and FF2, and between FF1 and FF3 when considering FF2 and FF3 hold time.

d. Does this circuit have a hold time problem? Justify you answer by analyzing al possible paths in your answer.

6. (Exercise 3.2, H&H RISC-V Edition) Given the input waveforms shown below, sketch the output, Q, of an SR latch.



7. (Exercise 3.3/3.5, H&H RISC-V Edition) Given the input waveforms shown below, sketch the output, Q of a D latch and of a D flip-flop.