Sequential Blocks

1. (Exercise 5.52 H&H RISC-V Edition) Build a 32-bity counter that add 4 at each clock edge. The counter has reset and clock inputs. Upon reset, the counter output is al 0.

2. Exercise 5.52 H&H RISC-V Edition) Build a 32-bity counter that will either increment by 4, or load a new 32-bit value D, on each clock edge, depending on a control signal *Load*. When *Load* = *1*, the counter loads the new value D. Otherwise it increments by 4.

3. (Exercise 5.54 H&H RISC-V Edition) An N-bit Johnson counter consists of an N-bit shift register with a reset signal. The output of the shift register S_{out} is inverted and fed back to the input S_{in}. When the counter is reset, all of the bits are cleared to 0.
    a. Show the sequence of outputs, $Q_{3:0}$ produced by a 4-bit Johnson counter starting immediately after the counter is reset.

    b. How many cycles elapse until an N-bit Johnson counter repeats its sequence? Explain.

c. Design a decimal counter using a 5-bit Johnson counter, ten AND gates, and inverters. The decimal counter has a clock, a reset, and ten one-hot output $Y_{9:0}$. When the counter is reset, Y_0 is asserted. On each subsequent cycle, the next output should be asserted. After ten cycles, the counter should repeat. Sketch a schematic of the decimal counter.

d. What advantages might a Johnson counter have over a conventional counter?

4. In Verilog, write a 4-port Read and 2-port Write Register File. Use the skeleton provided below. If the a read and write collision, prioritize reading the value before it has changed.

```
module RegisterFile (
  input  logic                clk,
  input  logic                reset,

  // Write port signals
  input  logic [1:0]          we,          // 2 write enables
  input  logic [4:0]          waddr[1:0],  // 5-bit write addresses for
32-depth
  input  logic [15:0]         wdata[1:0],  // 16-bit write data for 2
write ports

  // Read port signals
  input  logic [4:0]          raddr[3:0],  // 5-bit read addresses for 4
read ports
  output logic [15:0]         rdata[3:0]   // 16-bit read data for 4 read
ports
);
```

```
endmodule
```

5. Building from (4), this time write a parametrized N-port read and M-port write with Bypass collision handling. In bypass collision handling, if a port is being both read and written at the same time then the read should fetch the data begin written. The regfile is also parametrized on the DATA_WIDTH and has a depth of 32.

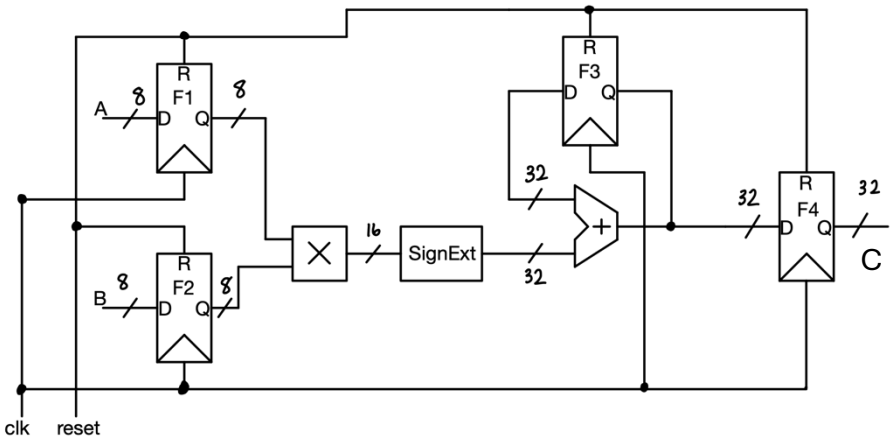
```
module RegisterFile #(
  parameter int DATA_WIDTH = 32,
  parameter int NUM_READ_PORTS = 4,
  parameter int NUM_WRITE_PORTS = 2,) (
  input  logic                      clk,
  input  logic                      reset,

  // Write port signals
  input  logic [NUM_WRITE_PORTS-1:0]                  we,          // Write enable
  input  logic [NUM_WRITE_PORTS*5-1:0]                waddr,       // 5-bit write
addresses (32-depth = 5-bit)
  input  logic [NUM_WRITE_PORTS*DATA_WIDTH-1:0]       wdata,       // Write data

  // Read port signals
  input  logic [NUM_READ_PORTS*5-1:0]                 raddr,       // 5-bit read
addresses
  output logic [NUM_READ_PORTS*DATA_WIDTH-1:0]        rdata        // Read data
);
```

```
endmodule
```

6. Consider the following 8-bit pipelined multiply-accumulate unit.



Gate	t_{pd}	Area
8-bit Multiplier	120τ	100α
16-to-32 SignExtend	60τ	30α
32-bit Adder	320τ	96α
8-bit FF	–	22α
16-bit FF	–	44α
32-bit FF	–	88α
8-bit FF Clock-to-Q	18τ	–
8-bit FF Setup	20τ	–
16-bit FF Clock-to-Q	36τ	–
16-bit FF Setup	40τ	–
32-bit FF Clock-to-Q	72τ	–
32-bit FF Setup	80τ	–
Input Clock-to-Port	0τ	–
Output Port Setup	0τ	–

Highlight one critical path on the block-level diagram above. Specify a critical path, the delay of each component on the path, and the corresponding path propagation delay in units of τ below. The path should be specified with modulate at the start of the path, the name of each module along the path, and the module at the end of the path. Use the constant delay and area models shown above.

Path	Delay of Each Component on Path	Path Delay

What is the minimum clock period (T_c), in units of τ?

What is the area in units α. Justify your answer below.