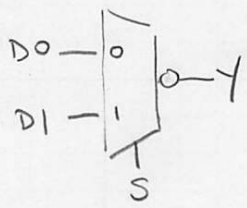
Activity

Implement an inverting 2-input multiplexer



Assume both S and $\overline{S}$ are available

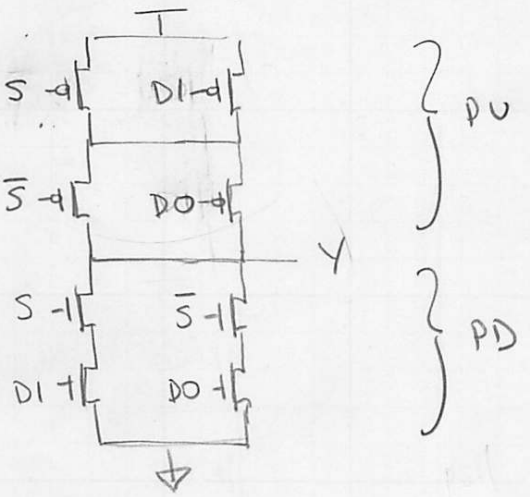
$$f = \overline{(S \cdot D1) + (\overline{S} \cdot D0)}$$

$$PD = (S \cdot D1) + (\overline{S} \cdot D0)$$

$$PU = \overline{(S \cdot D1) + (\overline{S} \cdot D0)}$$

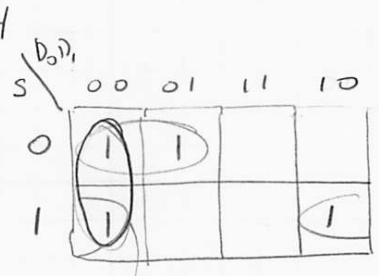
$$= \overline{(S \cdot D1)} \cdot \overline{(\overline{S} \cdot D0)}$$

$$= (\overline{S} + \overline{D1}) \cdot (S + \overline{D0})$$



IMPLEMENTATION 1

D_0	D_1	S	$\bar{Y}$	Y
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0



$$Y = \bar{D}_0\bar{D}_1\bar{S} + \bar{D}_0\bar{D}_1 S + \bar{D}_0 D_1\bar{S} + D_0\bar{D}_1 S$$ → SUM OF MINTERMS → K-MAP

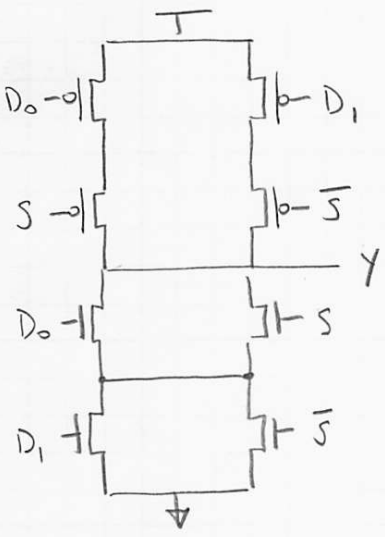
$$= \bar{D}_0\bar{S} + \bar{D}_1 S + \bar{D}_0\bar{D}_1$$ REDUNDANT

$$= \bar{D}_0\bar{S} + \bar{D}_1 S$$ → NEED EQUATION OF FORM $F = \overline{\text{SOMETHING}}$ SINCE STATIC CMOS IS INVERTING

$$= \overline{\bar{D}_0\bar{S} + \bar{D}_1 S}$$ → DEMORGAN'S

$$= \overline{(\bar{D}_0\bar{S})(\bar{D}_1 S)}$$

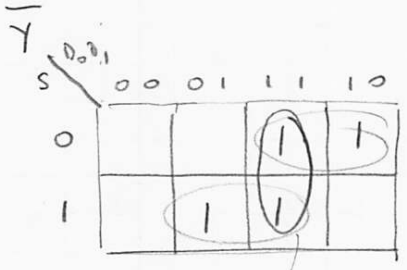
$$= (D_0 + S)(D_1 + \bar{S})$$



FOLLOWS STATIC CMOS DUALITY RULES

IMPLEMENTATION 2

D_0	D_1	S	$\overline{Y}$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

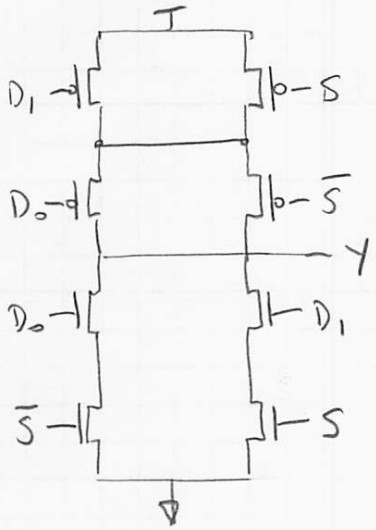


$$\overline{Y} = \overline{D}_0 D_1 S + D_0 \overline{D}_1 \overline{S} + D_0 D_1 \overline{S} + D_0 D_1 S$$ ← SUM OF MINTERMS

$$= D_0 \overline{S} + D_1 S + D_0 D_1$$ ← REDUNDANT ← KMAP

$$= D_0 \overline{S} + D_1 S$$ ← REALLY WANT TO IMPLEMENT Y NOT $\overline{Y}$

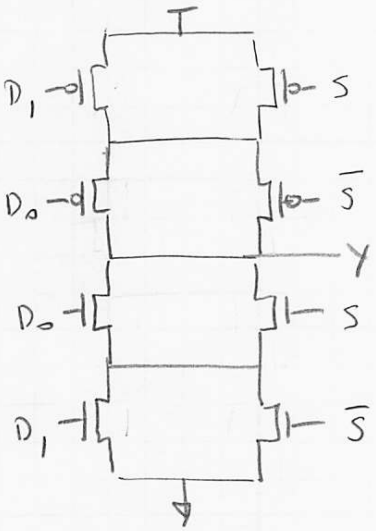
$$Y = \overline{D_0 \overline{S} + D_1 S}$$



FOLLOWS STATIC CMOS DUALITY RULES

IMPLEMENTATION 3

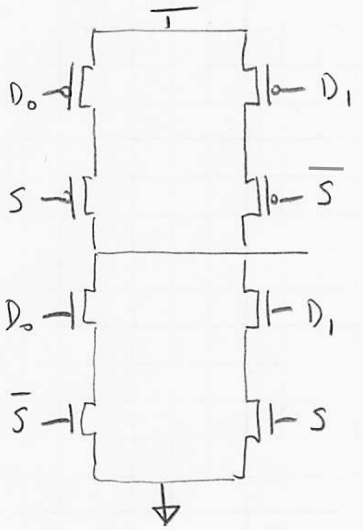
MIX PULL-DOWN FROM IMPL 1 W/ PULL-UP FROM IMPL 2



NOT DUALS OF EACH OTHER

IMPLEMENTATION 4

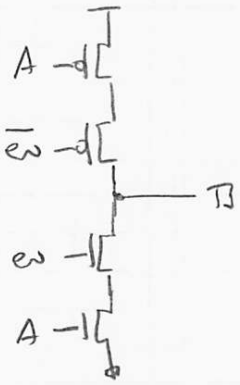
MIX PULL-UP FROM IMPL 1 W/ PULL-DOWN FROMP IMPL 2



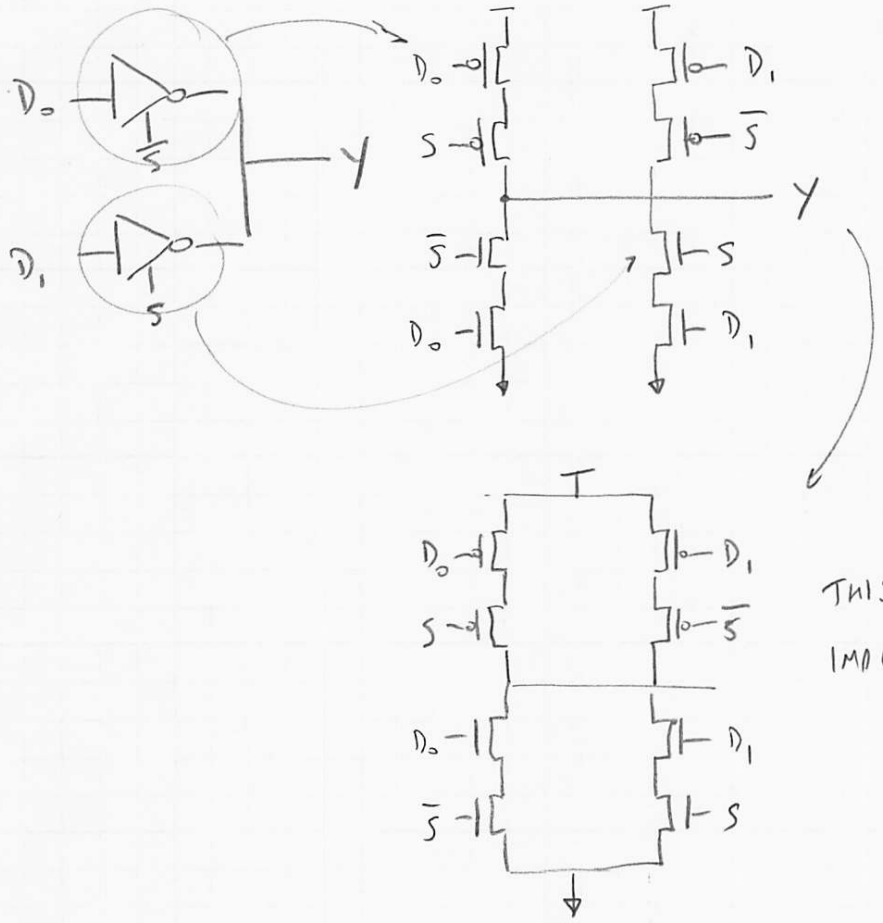
NOT DUALS OF EACH OTHER

IMPLEMENTATION 4 IS ESSENTIALLY A TRI-STATE MUX IMPL

TRISTATE BUFFER



TRISTATE MUX IMPL



THIS IS IMPL 4!

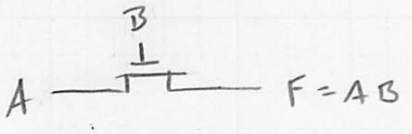
ACTIVITY

IMPLEMENT $F = ABC$ (3 INPUT AND GATE) USING PASS TRANSISTOR logic.

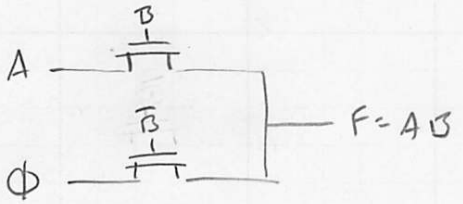
PASS TRANSISTORS CAN only "PASS" CAN ONLY BE A, B, C or their COMPLEMENT OR A CONSTANT ZERO. DON'T USE PASS TRANSISTORS TO "PASS" a CONSTANT VDD.

ENSURE THAT OUTPUT IS ALWAYS DRIVEN TO ϕ or VDD AND IS NEVER FLOATING.

START WITH 2 INPUT AND gate



BUT IF B=0, OUTPUT IS FLOATING



NOW OUTPUT IS ALWAYS DRIVEN HIGH or low

3 INPUT AND gate