Part 1: ASIC Design Overview

Topic 1: Hardware Description Languages

Topic 2: CMOS Devices

Topic 3: CMOS Circuits

Topic 4: Full-Custom Design Methodology

Topic 5: Automated Design Methodologies

Topic 6: Closing the Gap

Topic 7: Clocking, Power Distribution, Packaging, and I/O

Topic 8: Testing and Verification
Agenda

Packaging

Power Distribution

Clocking

I/O
Basic Approaches to Packaging

- Through-hole Mounted
- Surface Mounted
- Cavity-Up Pin Grid Array (PGA)
- Cavity-Down PGA
- Ball Grid Array (BGA)

- Solder bumps placed on top of pads across die area
- Chip flipped onto package and solder balls reflowed

IBM C4 - Controlled Collapse Chip Connection

Adapted from [Terman'02]
Basic Package Types

What makes a good package?

- Low cost
- Small size
- Good thermal performance

- Large number of pins
- Low pin parasitics
- Easy to test
- Highly reliable

Adapted from [Weste’11]
## Basic Package Types

<table>
<thead>
<tr>
<th>Type</th>
<th>Quantity</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP</td>
<td>8–64</td>
<td>Two rows of through-hole pins. 100mil pitch. Low cost. Long wires between chip and corner pins.</td>
</tr>
<tr>
<td>PGA</td>
<td>65-400</td>
<td>Array of through-hole pins. 100mil pitch. Low thermal resistance and higher pin counts.</td>
</tr>
<tr>
<td>SOIC</td>
<td>8–28</td>
<td>Two rows of SMT pins. 50mil pitch. Low cost.</td>
</tr>
<tr>
<td>TSOP</td>
<td>28–86</td>
<td>Two rows of SMT pin. 0.5–0.8mil pitch in thin package. Used in DRAMs.</td>
</tr>
<tr>
<td>QFP</td>
<td>44–240</td>
<td>SMT pins on 4 sides. 15–50mil pitch. High density.</td>
</tr>
<tr>
<td>LGA</td>
<td>Many</td>
<td>Similar to BGA but with gold pads instead of solder balls. Commonly used with sockets (processors).</td>
</tr>
</tbody>
</table>

Adapted from [Weste’11]
Wire-Bond Pad Ring
Wire Bonding Process

- Usually ultrasonic welding connects wire to package and die pad
- Bond wires can be aluminum or gold
- Different thicknesses of bond wire tradeoff parasitic inductance and resistance versus density
- Can wirebond to die pad pitches of around 100μm

Adapted from [Terman'02]
Pin-Grid Array Assembly Process

- Tested Wafer
- Saw
- Die
- Die Attach (glue to package)
- Oven Cure Die Attach
- Wire bond pads on die to pads on package
- Glue lid on package
- Oven Cure Lid Attach
- Final Test
- Screen Printing

Adapted from [Terman'02]
Summary of Package Parasitics

Adapted from [Weste’11]
Pin Parasitics

Wire bond, $C_{\text{bond}}=1\,\text{pF}$, $L_{\text{bond}}=1\,\text{nH}$
- bond wire $L$ approx. $1\,\text{nH/mm}$
Solder bump, $C_{\text{bond}}=0.5\,\text{pF}$, $L_{\text{bond}}=0.1\,\text{nH}$

68-pin DIP, $C_{\text{pin}}=4\,\text{pF}$, $L_{\text{pin}}=35\,\text{nH}$
256-pin PGA, $C_{\text{pin}}=3-5\,\text{pF}$, $L_{\text{pin}}=5-15\,\text{nH}$
BGA, $C_{\text{pin}}=2-4\,\text{pF}$, $L_{\text{pin}}=1-8\,\text{nH}$

Adapted from [Terman'02]
Challenge: Power Delivery Scaling

Power = Volts $\times$ Amps

- CPU power consumption is increasing
  - 2x per technology generation

- Supply voltages are dropping
  - have to control electric field strength as transistors shrink
  - keep power from growing even faster

- Power is going up, voltage is going down = current rising fast
  - 100W at 1V implies 100A of current
**Challenge: Static IR Droop**

Want to keep voltage droop ($V = IR$) small

Example, for 100W@1V, $I=100A$
- 5% droop is 50mV
- At 100A, need effective supply resistance $< 0.0005 \, \Omega$
- Dissipate 5W heat just in power supply leads

- Use multiple parallel Vdd/GND pins
- Need very short fat wires to board power regulator
- Want very low resistance on-chip power network

Adapted from [Terman’02]
Challenge: Dynamic $dI/dt$ Droop

- A large number of output drivers $A$ switching high try to pull current through the power supply inductance, causing the internal power rail connected to gate $B$ to droop ($V=LI/dt$)
- Gates driven by $B$ may switch incorrectly.

Adapted from [Terman’02]
Challenge: Heat Dissipation

Sample overall $\theta_{ja}$:
- DIP $38^\circ C/W$ still air
- DIP $25^\circ C/W$ forced air
- PGA $5-10^\circ C/W$ forced air
- Microproc. and fan $<3^\circ C/W$
  (fluid pumped through die microchannels $0.02^\circ C/W$)

Adapted from [Terman'02]
Agenda

Packaging

Power Distribution

Clocking

I/O
Power Distribution Network Parasitics

Possible IR drop across power network:

\[ \text{VDD} \rightarrow \text{GND} \]

\[ \begin{align*}
R_{\text{eff}} & \quad C_g \\
& \quad R_{\text{eff}} \\
& \quad C_d \\
& \quad R_{\text{eff}} \\
& \quad C_d
\end{align*} \]

\[ \text{VDD} \rightarrow \text{GND} \]
Static and Dynamic IR Drop

IR drop can be static or dynamic.

\[ V_{DD} \rightarrow R_{eff} \rightarrow C_g \rightarrow R_{eff} \rightarrow C_d \rightarrow V_{DD} \]

Are these parasitic capacitances bad?
Realistic Power Distribution Networks

Adapted from [Weste’11]
Various Approaches to Power Distribution

Routed power distribution on two stacked layers of metal (one for VDD, one for GND). OK for low-cost, low-power designs with few layers of metal.

Power Grid. Interconnected vertical and horizontal power bars. Common on most high-performance designs. Often well over half of total metal on upper thicker layers used for VDD/GND.

Power Distribution for Standard Cells

Adapted from [Weste’11]
Modular Power Distribution Networks

- Power Distribution
- Clocking
- I/O

Power rings partition the power problem.

Early physical partitioning and prototyping is essential.

Can use special filler cells to help add decoupling cap.
Fine-grain power distribution grid over entire chip reduces IR drop issues. Fine-grained grid ensures adequate power delivery and the automatic router handles many small blockages better than fewer large blockages.
Agenda

Packaging
Power Distribution
Clocking
I/O
Goal of Clock Distribution

Clock Distribution: The Issue

Clock propagates across entire chip

Clock cannot really distribute clock instantaneously with a perfectly regular period.
Clock Skew

Difference in clock arrival time at two spatially distinct points
Clock Jitter

Difference in clock period over time

Period A ≠ Period B
Sources of Clock Skew and Jitter

Variations in trace length, metal width and height, coupling caps

Variations in local clock load, local power supply, local gate length and threshold, local temperature

Central Clock Driver

Clock Distribution Network

Local Clock Buffers
Clock Grids: Low Skew but High Power

Clock driver tree spans height of chip
Internal levels shorted together

Grid feeds flops directly, no local buffers
Clock Trees: More skew but Less Power

H-Tree

Recursive pattern to distribute signals uniformly with equal delay over area

RC-Tree

Each branch is individually routed to balance RC delay
Clock Tree Synthesis

CAD tools generate balanced RC trees

Static analysis to measure clock skew and factor it into static timing analysis
Example Skew/Jitter Analysis

The physical view of a clock tree

Adapted from [Xiu'08]
Example Skew/Jitter Analysis

Adapted from [Xiu’08]
Active Deskewing Circuits in Intel Itanium

Active Deskew Circuits (cancels out systematic skew)

Phase Locked Loop (PLL)

Regional Grid
Agenda

Packaging

Power Distribution

Clocking

I/O
Single-Ended I/O Standards

- **V_{CC}:** Input High level Voltage
- **V_{LL}:** Input Low level Voltage
- **V_{OH}:** Output High level Voltage
- **V_{OL}:** Output Low level Voltage
- **V_{TH}:** Threshold Voltage

Adapted from [www.interfacebus.com]
I/O Pads

Adapted from [Weste’11]
High-Speed Serial I/Os

- Pins are an expensive part of a system
  - Physical cost of adding pin to package
  - Size of package increases with more pins and on-pkg routing to pin
  - Bonding cost per pin
  - Size of motherboard depends on package size
  - More pins complicates board-level routing
  - Board testing time grows with number of pins
  - Reliability is function of number of solder connections

- Trend towards high-speed serial I/O
  - As computing performance grows, pins become system bottleneck
  - Want maximum bandwidth from available pins
  - Current SerDes run at 3–6 Gb/s per link at <200 mW
Acknowledgments


