PROCESSORS FIRST-ORDER ANALYSIS

$$\frac{\text{TIME}}{\text{PROGRAM}} = \frac{\text{INSTRUCTIONS}}{\text{PROGRAM}} \times \frac{\text{CYCLES}}{\text{INSTRUCTION}} \times \frac{\text{TIME}}{\text{CYCLES}}$$

QUANTITATIVE (PIPELINE DIAGRAMS, RTL)

QUALITATIVE

MEMORIES FIRST-ORDER ANALYSIS

$$\text{AVG MEM ACCESS LATENCY} = \text{HIT TIME} + (\text{MISS RATE} \times \text{MISS PENALTY})$$

QUANTITATIVE (IN TERMS OF CYCLES)

QUANTITATIVE

QUANTITATIVE

NETWORKS FIRST-ORDER ANALYSIS

$$\text{IDEAL TERMINAL THROUGHPUT} = \frac{\text{CHANNEL BANDWIDTH}}{\text{MAX CHANNEL LOAD}}$$

QUANTITATIVE (BITS / CYCLE)

QUANTITATIVE

$$\text{ZERO LOAD LATENCY} = \left(\text{ROUTER HOPS} \times \text{ROUTER LATENCY}\right) + \left(\text{CHANNEL HOPS} \times \text{CHANNEL LATENCY}\right) + \frac{\text{BITS / MSG}}{\text{BITS / CYCLE}}$$

QUANTITATIVE (CYCLES)

QUALITATIVE ASSUMPTIONS

1. AREA — μm^2
2. CYCLE TIME — ns
3. ENERGY — J

ECE 5745 Complex Digital ASIC Design

Activity 1: Integer Multipler

Problem 1. Quantitative Evaluation of Integer Multiplier Microarchitectures

Consider two integer multiplier microarchitectures similar to the designs you studied in ECE 4750. Both multipliers are capable of multiplying a 32-bit operand by a 4-bit operand to produce a truncated 32-bit result.

The first microarchitecture is a fixed-latency iterative multiplier which always requires four cycles to calculate the result. The second microarchitecture is a variable-latency iterative multiplier which exploits the fact that when some of the bits in the four-bit operand are zero, we don't actually have to do any work. In the variable-latency design, the number of cycles to calculate the result is proportional to the number of ones in the four-bit operand.

For all parts in this problem assume that our multiplier is processing the following sequence of four independent transactions.

```
1 mul 0xdeadbeef, 0xf
2 mul 0xf5fe4fbc, 0x7
3 mul 0x0a01b044, 0x3
4 mul 0x0a01b044, 0x1
```

Part 1.A Execution Time in Cycles for Fixed-Latency Iterative Multiplier Microarchitecture

Draw a pipeline diagram illustrating the execution of the four multiplication transactions on the fixed-latency iterative multiplier microarchitecture. Denote each cycle a transaction is in the iterative multiplier with the symbol Z. **Calculate the total execution time in cycles to execute the transaction sequence.**

`mul 0xdeadbeef, 0xf`																	
`mul 0xf5fe4fbc, 0x7`																	
`mul 0x0a01b044, 0x3`																	
`mul 0x0a01b044, 0x1`																	

Part 1.B Execution Time in Cycles for Variable-Latency Iterative Multiplier Microarchitecture

Draw a pipeline diagram illustrating the execution of the four multiplication transactions on the variable-latency iterative multiplier microarchitecture. Denote each cycle a transaction is in the iterative multiplier with the symbol Z. **Calculate the total execution time in cycles to execute the transaction sequence.**

`mul 0xdeadbeef, 0xf`																	
`mul 0xf5fe4fbc, 0x7`																	
`mul 0x0a01b044, 0x3`																	
`mul 0x0a01b044, 0x1`																	

Problem 2. Qualitative Evaluation of Integer Multiplier Microarchitectures

In addition to the two microarchitectures described in the previous problem, consider a single-cycle combinational multiplier and a (fixed-latency) four-stage pipelined multiplier for a total of four multiplier microarchitectures. Qualitatively compare the four microarchitectures in terms of their area (μm^2), cycle time (ns), total execution time (cycles), and total energy (Joules). Your ranking should be for the specific sequence of multiplication transactions considered in the previous problem.

Fill in the table below with a relative ranking for each microarchitecture; a rank of 1 means that design is relatively the "best" in terms of the corresponding metric (i.e., least area, shortest cycle time, shortest execution time, least energy) and a rank of 4 means that design is the relatively the "worst" in terms of the corresponding metric (i.e., most area, longest cycle time, longest execution time, most energy). Feel free to give two microarchitectures the same rank if they would be comparable in terms of the corresponding metric.

Microarchitecture	**Area (μm^2)**	**Cycle Time (ns)**	**Tot Exec Time (cycles)**	**Tot Energy (Joules)**
Fixed-Latency Iterative				
Variable-Latency Iterative				
Single-Cycle Combinational				
4-Stage Pipelined				