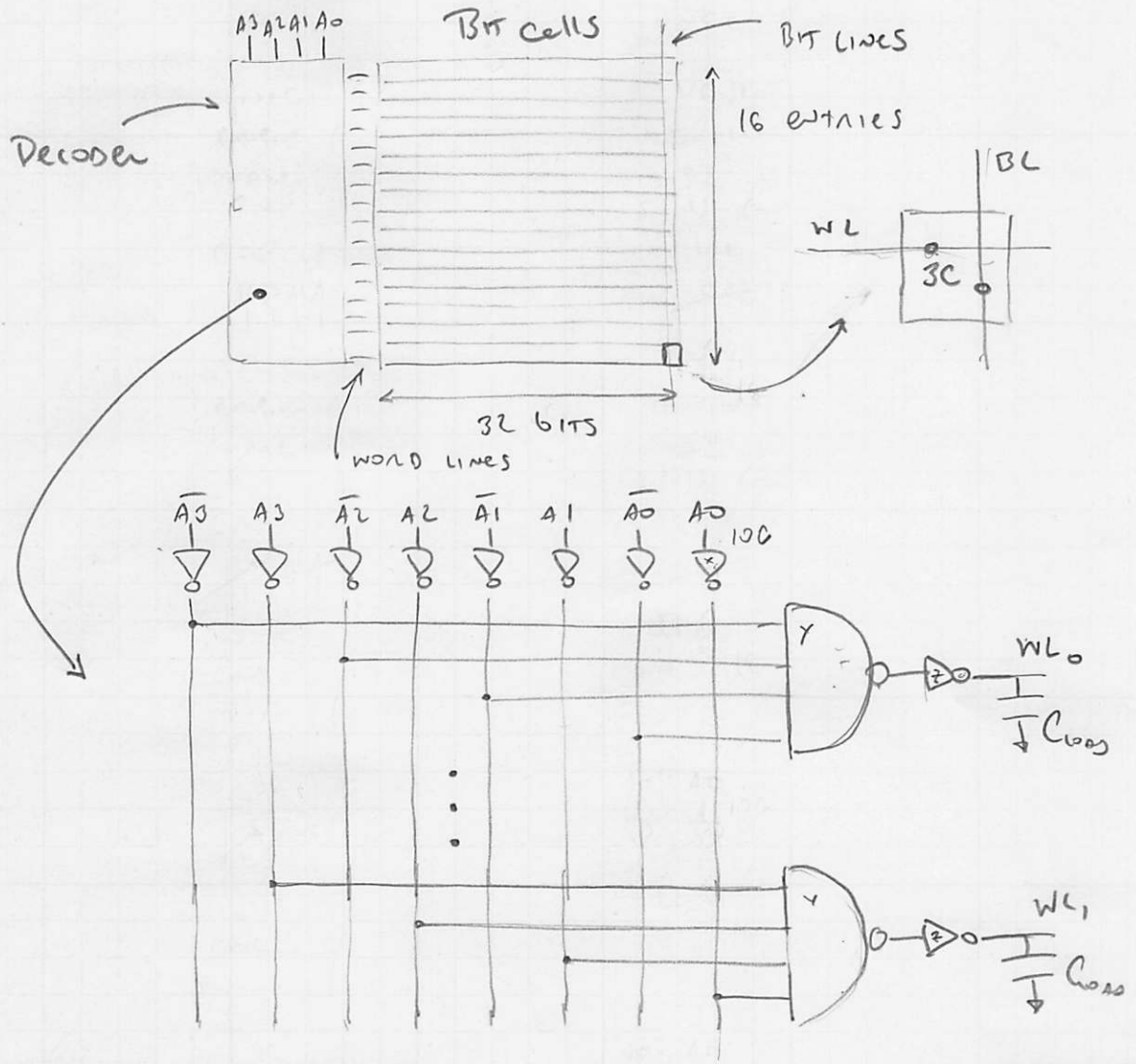
Problem 1

Consider a decoder suitable for use in a 16 entry register file where every entry is 32 bits wide

Assume gate cap for the word enable signal in each cell is 3C. Ignore interconnect capacitance

Assume both true and complement versions of the address bits are available.

Assume input cap for address bits is constrained to 10C

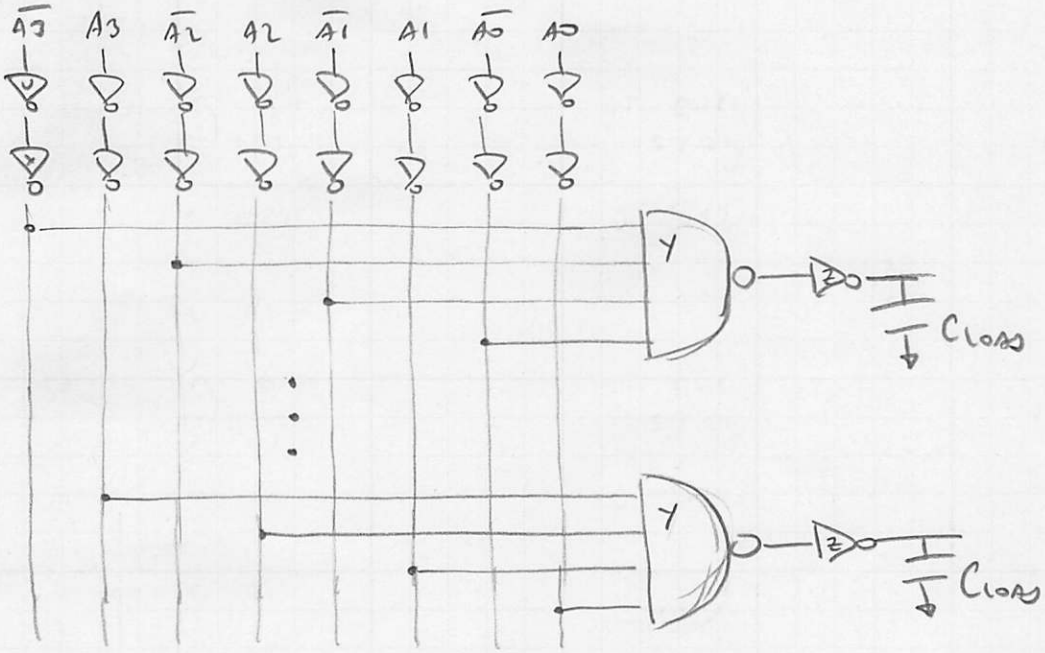


A. What is optimal delay?
B. What is optimal sizing?
C. What is (roughly) optimal number of stages?
D What is total switched cap?

Problem 2

Consider adding another inverter at every address bit to increase the total number of stages to four

Recalculate the optimal delay and sizing



Compare this optimal delay and sizing to the three stage design

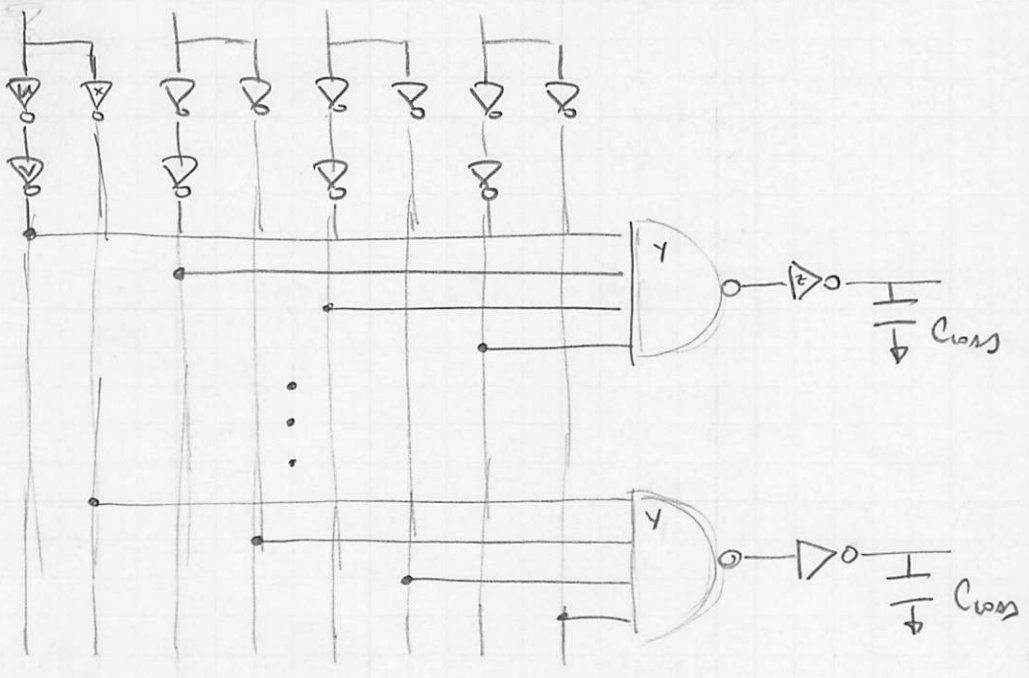
Problem 3

Consider situation where address bits are only available in true polarity and we must generate complement signal locally

Assume input cap for true address bit is constrained to 20c. Assume we evenly divide this cap across both inverters at the input branch

The sizing for the 3-stage and 4-stage do not match. Assume we keep 3-stage sizing for Y and Z gates.

How do we size inverter Y? We want delay through the single inv and double inv branches of the "fork" to be equal



Calculate the critical path which will be either through the single inverter or double inverter branch