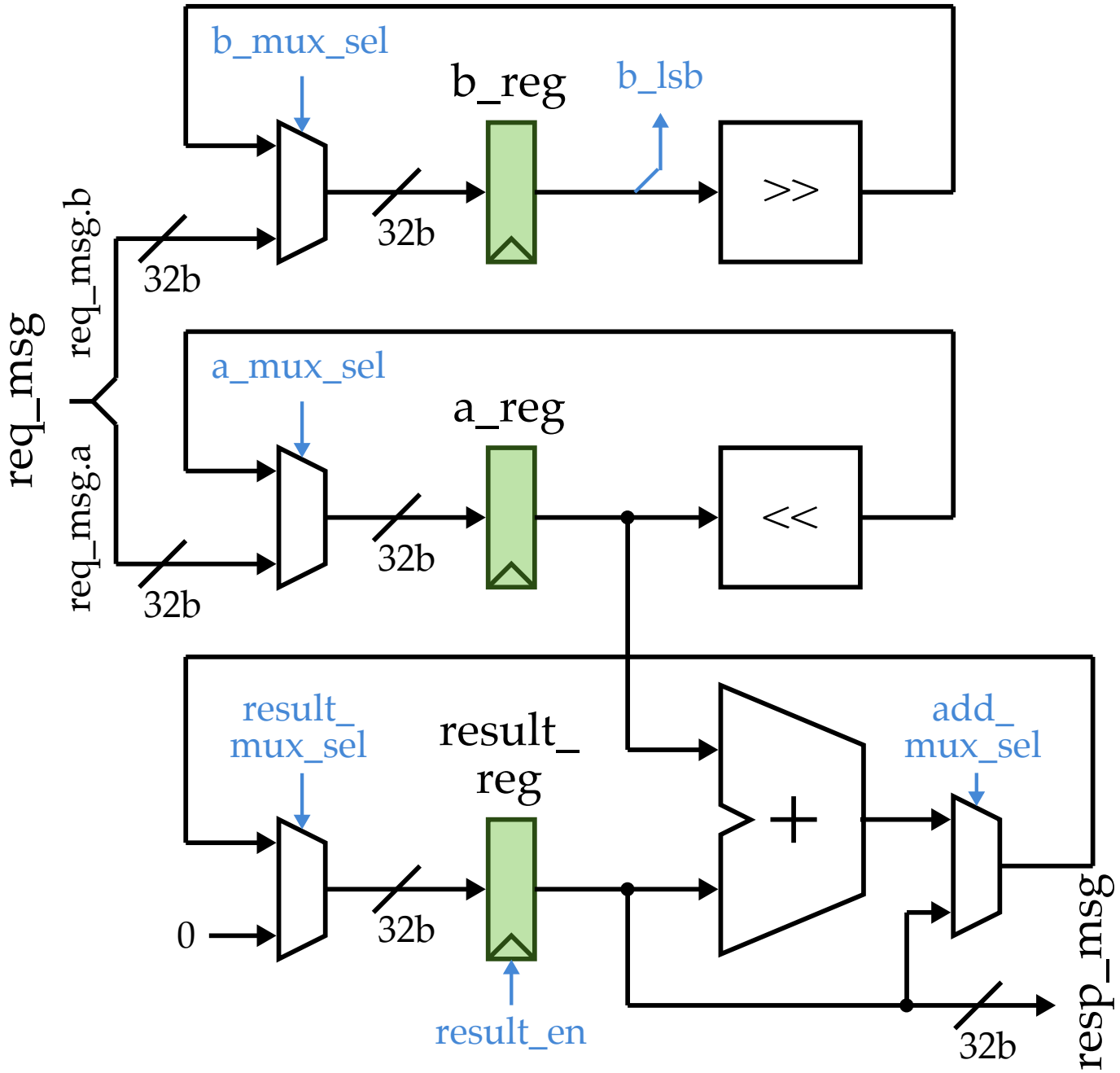
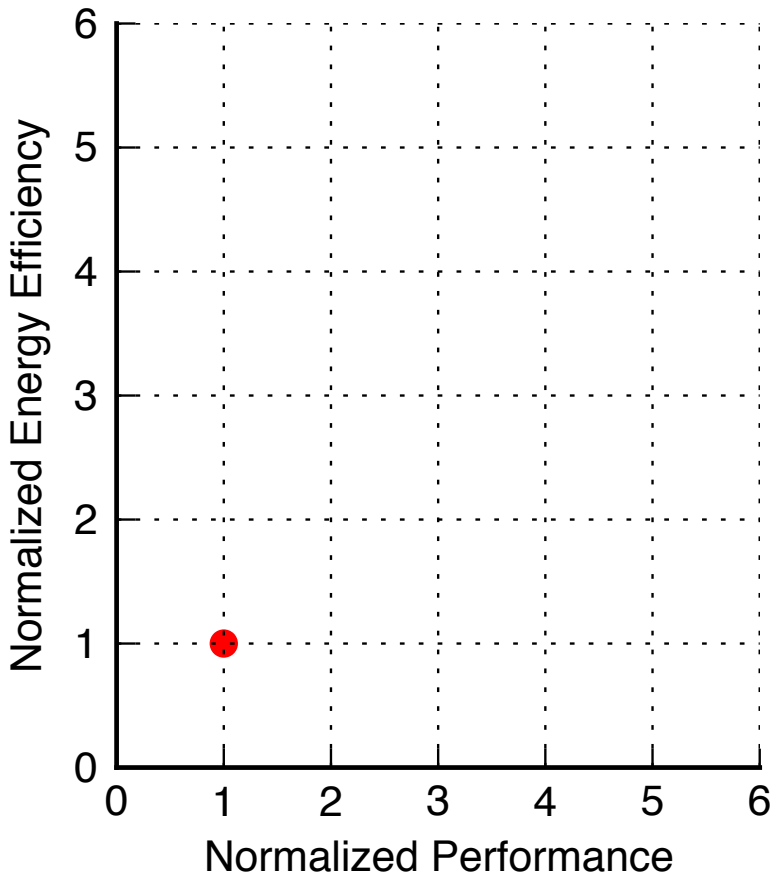
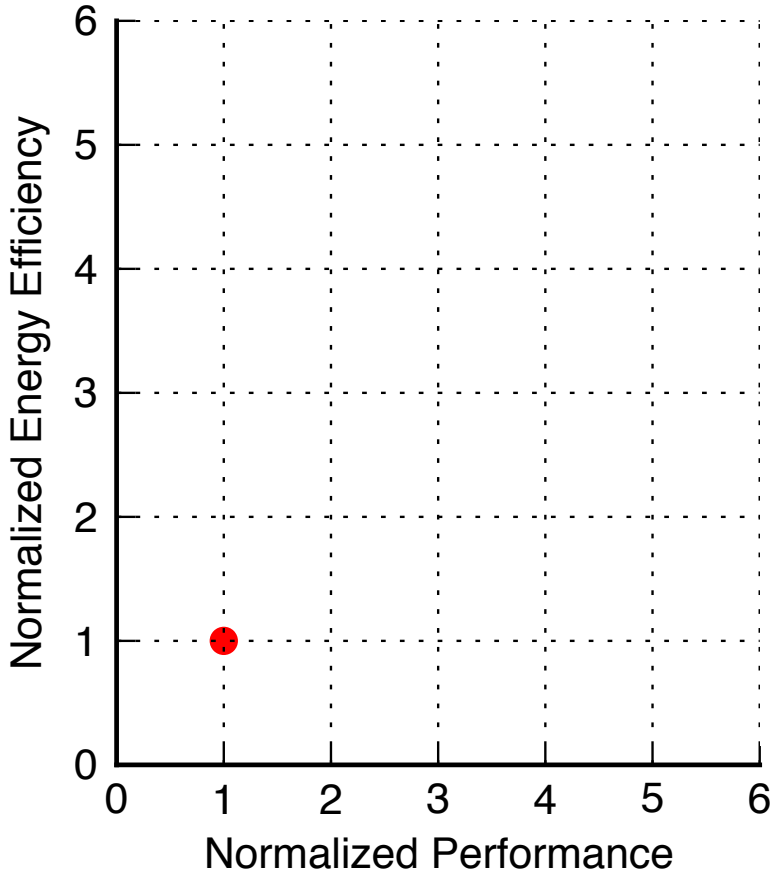
```
Point                                          Fanout       Cap     Trans      Incr       Path
  ------------------------------------------------------------------------------------------------
  clock ideal_clock1 (rise edge)                                                0.0000     0.0000
  clock network delay (propagated)                                              0.1797     0.1797
  dpath/result_reg/out_reg_12_/CLK (DFFX1)                            0.1627    0.0000     0.1797 r
  dpath/result_reg/out_reg_12_/Q (DFFX1)                              0.0579    0.2249     0.4046 f
  dpath/result_reg/out[12] (net)                 4      14.7511               0.0000     0.4046 f
  dpath/result_reg/out[12] (RegEn_0x5d7f49276b3a51fc)                           0.0000     0.4046 f
  dpath/resp_msg[12] (net)                              14.7511               0.0000     0.4046 f
  dpath/add/in1[12] (Adder_0x5e7f7d3cd3d8940e)                                  0.0000     0.4046 f
  dpath/add/in1[12] (net)                               14.7511               0.0000     0.4046 f
  dpath/add/U79/IN1 (NAND2X0)                                         0.0579    0.0002 &   0.4048 f
  dpath/add/U79/QN (NAND2X0)                                          0.0984    0.0563     0.4610 r
  dpath/add/n293 (net)                           3       7.3223               0.0000     0.4610 r
  dpath/add/U81/IN1 (OAI21X1)                                         0.0984    0.0022 &   0.4633 r
  dpath/add/U81/QN (OAI21X1)                                          0.0391    0.1213     0.5845 f
  dpath/add/n304 (net)                           3       8.0761               0.0000     0.5845 f
  dpath/add/U85/IN1 (AOI21X1)                                         0.0391    0.0000 &   0.5845 f
  dpath/add/U85/QN (AOI21X1)                                          0.0300    0.0968     0.6813 r
  dpath/add/n23 (net)                            1       3.7021               0.0000     0.6813 r
  dpath/add/icc_clock4/IN3 (NAND3X0)                                  0.0300    0.0000 &   0.6814 r
  dpath/add/icc_clock4/QN (NAND3X0)                                   0.0815    0.0489     0.7303 f
  dpath/add/n32 (net)                            1       8.9536               0.0000     0.7303 f
  dpath/add/icc_clock5/INP (INVX2)                                    0.0815    0.0000 &   0.7303 f
  dpath/add/icc_clock5/ZN (INVX2)                                     0.0988    0.0606     0.7909 r
  dpath/add/n199 (net)                          16      50.2237               0.0000     0.7909 r
  dpath/add/U157/IN2 (OAI21X1)                                        0.0988    0.0010 &   0.7920 r
  dpath/add/U157/QN (OAI21X1)                                         0.0361    0.1083     0.9002 f
  dpath/add/n74 (net)                            1       6.9548               0.0000     0.9002 f
  dpath/add/icc_clock3/IN1 (XNOR2X1)                                  0.0361    0.0014 &   0.9016 f
  dpath/add/icc_clock3/Q (XNOR2X1)                                    0.0508    0.1185     1.0201 r
  dpath/add/out[31] (net)                        1       6.8784               0.0000     1.0201 r
  dpath/add/out[31] (Adder_0x5e7f7d3cd3d8940e)                                  0.0000     1.0201 r
  dpath/add_out[31] (net)                               6.8784               0.0000     1.0201 r
  dpath/add_mux/in__000[31] (Mux_0x4543312b8315d283_3)                          0.0000     1.0201 r
  dpath/add_mux/in__000[31] (net)                       6.8784               0.0000     1.0201 r
  dpath/add_mux/U3/IN1 (NAND2X2)                                      0.0508    0.0000 &   1.0202 r
  dpath/add_mux/U3/QN (NAND2X2)                                       0.0963    0.0209     1.0410 f
  dpath/add_mux/n2 (net)                         1       3.6708               0.0000     1.0410 f
  dpath/add_mux/U6/IN1 (NAND2X1)                                      0.0963    0.0000 &   1.0410 f
  dpath/add_mux/U6/QN (NAND2X1)                                       0.0787    0.0364     1.0774 r
  dpath/add_mux/out[31] (net)                    1       4.5321               0.0000     1.0774 r
  dpath/add_mux/out[31] (Mux_0x4543312b8315d283_3)                              0.0000     1.0774 r
  dpath/add_mux_out[31] (net)                           4.5321               0.0000     1.0774 r
  dpath/result_mux/in__000[31] (Mux_0x4543312b8315d283_0)                       0.0000     1.0774 r
  dpath/result_mux/in__000[31] (net)                    4.5321               0.0000     1.0774 r
  dpath/result_mux/U4/INP (INVX1)                                     0.0787    0.0000 &   1.0774 r
  dpath/result_mux/U4/ZN (INVX1)                                      0.0381    0.0271     1.1045 f
  dpath/result_mux/n35 (net)                     1       5.2324               0.0000     1.1045 f
  dpath/result_mux/U5/IN1 (NOR2X2)                                    0.0381    0.0000 &   1.1045 f
  dpath/result_mux/U5/QN (NOR2X2)                                     0.0726    0.0215     1.1260 r
  dpath/result_mux/out[31] (net)                 1       3.0392               0.0000     1.1260 r
  dpath/result_mux/out[31] (Mux_0x4543312b8315d283_0)                           0.0000     1.1260 r
  dpath/result_mux_out[31] (net)                        3.0392               0.0000     1.1260 r
  dpath/result_reg/in_[31] (RegEn_0x5d7f49276b3a51fc)                           0.0000     1.1260 r
  dpath/result_reg/in_[31] (net)                        3.0392               0.0000     1.1260 r
  dpath/result_reg/out_reg_31_/D (DFFX1)                              0.0726    0.0000 &   1.1260 r
  data arrival time                                                                        1.1260

  clock ideal_clock1 (rise edge)                                                1.0000     1.0000
  clock network delay (propagated)                                              0.1761     1.1761
  clock reconvergence pessimism                                                 0.0006     1.1768
  dpath/result_reg/out_reg_31_/CLK (DFFX1)                                      0.0000     1.1768 r
  library setup time                                                           -0.0564     1.1204
  data required time                                                                       1.1204
  ------------------------------------------------------------------------------------------------
  data required time                                                                       1.1204
  data arrival time                                                                       -1.1260
  ------------------------------------------------------------------------------------------------
  slack (VIOLATED)                                                                        -0.0056
```


b_mux_sel
b_reg
b_lsb
>>
32b
32b
req_msg.b
req_msg
req_msg.a
a_mux_sel
a_reg
<<
32b
32b
result_
mux_sel
result_
reg
add_
mux_sel
+
0
32b
result_en
32b
resp_msg

```
vsrc       = IntMulFixedLatPRTL_0x791afe0d4d8c.v
input      = imul-rtl-fixed-small
area       = 9178 # um^2
constraint = 1.0 # ns
slack      = -0.01 # ns
cycle_time = 1.01 # ns
exec_time  = 1705 # cycles
power      = 3.958 # mW
energy     = 6.8158739 # nJ

vsrc       = IntMulFixedLatPRTL_0x791afe0d4d8c.v
input      = imul-rtl-fixed-large
area       = 9178 # um^2
constraint = 1.0 # ns
slack      = -0.01 # ns
cycle_time = 1.01 # ns
exec_time  = 1705 # cycles
power      = 6.532 # mW
energy     = 11.2484306 # nJ

vsrc       = IntMulVarLatPRTL_0x791afe0d4d8c.v
input      = imul-rtl-var-small
area       = 13300 # um^2
constraint = 1.0 # ns
slack      = -0.01 # ns
cycle_time = 1.01 # ns
exec_time  = 398 # cycles
power      = 5.231 # mW
energy     = 2.10275738 # nJ

vsrc       = IntMulVarLatPRTL_0x791afe0d4d8c.v
input      = imul-rtl-var-large
area       = 13300 # um^2
constraint = 1.0 # ns
slack      = -0.01 # ns
cycle_time = 1.01 # ns
exec_time  = 1371 # cycles
power      = 7.536 # mW
energy     = 10.43517456 # nJ
```



Energy Efficiency vs. Performance for Small Random Inputs



Energy Efficiency vs. Performance for Large Random Inputs

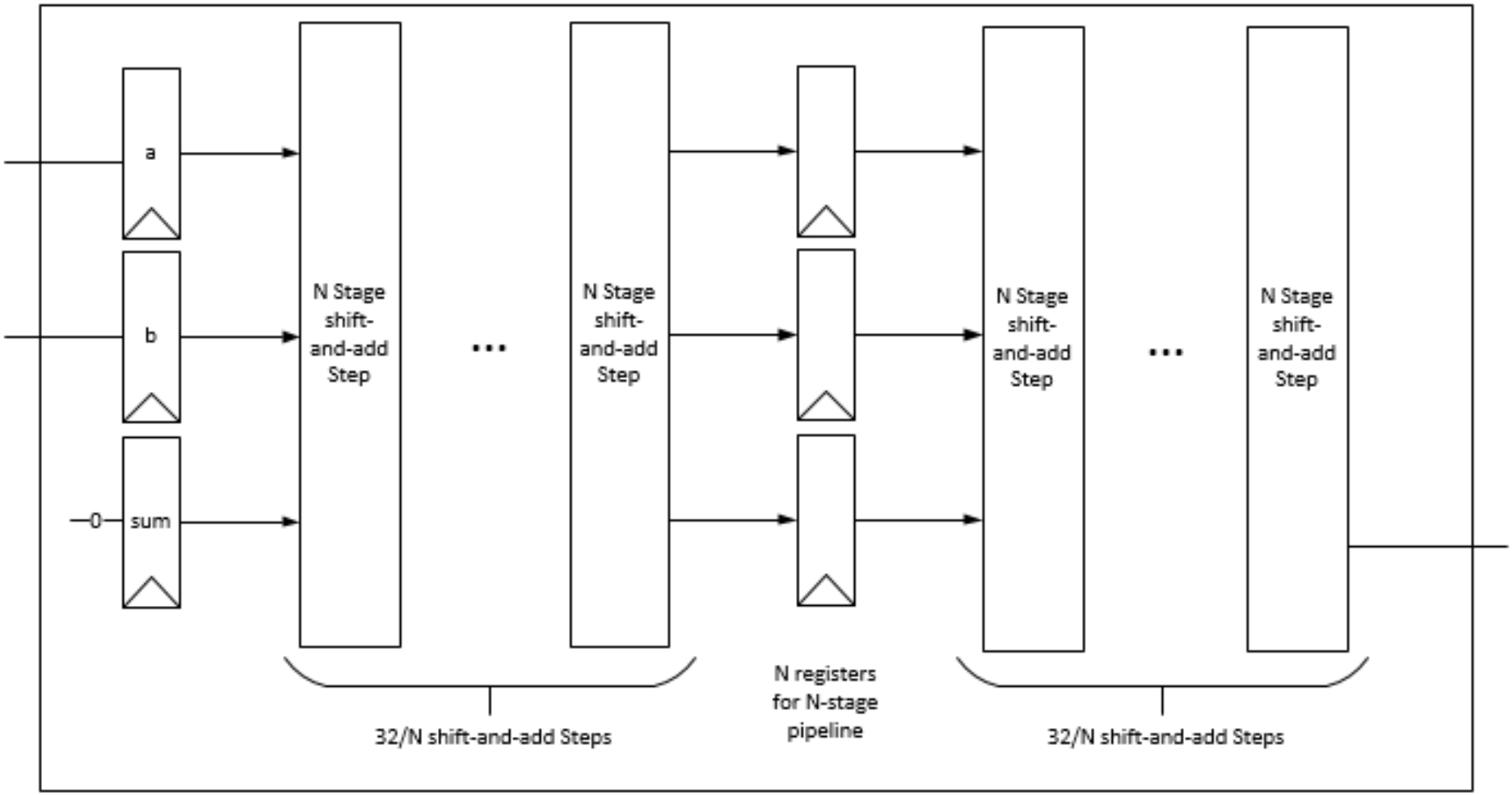


Figure 3.1 - N-stage Pipelined Multiplier: This multiplier consists of a variable number of stages based on an input parameter. Each stage is bookended by registers, and a stage consists of 32/N shift-and-add steps (see **Figure 3.2** below). The pipelining allows multiple multiplication operations to being partially computed each cycle in different stages of the multiplier to allow a throughput of 1 multiplication operation per cycle ideally.

```
../lab1-imul/IntMulNstageInelasticRTL_test.py::test_8stage ()
  2:                    >                    [........]          >
  3:                    >                    [........]          >
  4: 00000001:0000002f > 00000001:0000002f [........]          >
  5:                    >                    [1.......]          >
  6: 0000003c:0000002b > 0000003c:0000002b [.1......]          >
  7:                    >                    [1.1.....]          >
  8: 0000003d:00000049 > 0000003d:00000049 [.1.1....]          >
  9:                    >                    [1.1.1...]          >
 10:                    >                    [.1.1.1..]          >
 11: 0000003f:00000061 > 0000003f:00000061 [..1.1.1.]          >
 12:                    >                    [1..1.1.1] 0000002f > 0000002f
 13: #                  > #                  [.1..1.1.] .        > .
 14: #                  > #                  [.1..1.1.] .        > .
 15: #                  > #                  [.1..1.1.] .        > .
 16: #                  > #                  [.1..1.1.] .        > .
 17: #                  > #                  [.1..1.1.] .        > .
 18: #                  > #                  [.1..1.1.] .        > .
 19: 00000021:00000024 > 00000021:00000024 [.1..1.1.]          >
 20:                    >                    [1.1..1.1] 00000a14 > 00000a14
 21: .                  > .                  [.1.1..1.] .        > .
 22: .                  > .                  [.1.1..1.] .        > .
 23: #                  > #                  [.1.1..1.] .        > .
 24: #                  > #                  [.1.1..1.] .        > .
 25: #                  > #                  [.1.1..1.] .        > .
 26: #                  > #                  [.1.1..1.] .        > .
 27: #                  > #                  [.1.1..1.] .        > .
 28: #                  > #                  [.1.1..1.] .        > .
 29: #                  > #                  [.1.1..1.] .        > .
 30: 00000043:00000049 > 00000043:00000049 [.1.1..1.]          >
 31:                    >                    [1.1.1..1] 00001165 > 00001165
 32: .                  > .                  [.1.1.1..] .        > .
 33: .                  > .                  [.1.1.1..] .        > .
 34: #                  > #                  [.1.1.1..] .        > .
 35: #                  > #                  [.1.1.1..] .        > .
 36: #                  > #                  [.1.1.1..] .        > .
 37: #                  > #                  [.1.1.1..] .        > .
 38: 00000052:00000026 > 00000052:00000026 [.1.1.1..]          >
 39:                    >                    [1.1.1.1.]          >
 40:                    >                    [.1.1.1.1] 000017df > 000017df
 41: .                  > .                  [..1.1.1.] .        > .
 42: 00000033:0000001b > 00000033:0000001b [..1.1.1.]          >
 43:                    >                    [1..1.1.1] 000004a4 > 000004a4
 44: #                  > #                  [.1..1.1.] .        > .
```

Figure 4.4 - Trace for Inelastic 8-stage Pipelined Multiplier: The eight dots/ones in the square brackets specify in the value in the stage is invalid/valid. Notice that when the output is not ready (denoted with a dot on the right-most column), the pipeline does not have any valid computations progressing anywhere in the pipeline.

```
../lab1-imul/IntMulNstageRTL_test.py::test_8stage ()
 2:                    >                    [........]          >
 3:                    >                    [........]          >
 4: 00000001:0000002f > 00000001:0000002f [........]          >
 5:                    >                    [1.......]          >
 6: 0000003c:0000002b > 0000003c:0000002b [.1......]          >
 7:                    >                    [1.1.....]          >
 8: 0000003d:00000049 > 0000003d:00000049 [.1.1....]          >
 9:                    >                    [1.1.1...]          >
10:                    >                    [.1.1.1..]          >
11: 0000003f:00000061 > 0000003f:00000061 [..1.1.1.]          >
12:                    >                    [1..1.1.1] 0000002f > 0000002f
13: 00000021:00000024 > 00000021:00000024 [.1..1.1.] .        > .
14:                    >                    [1.1..1.1] #        > #
15:                    >                    [.1.1..11] #        > #
16: 00000043:00000049 > 00000043:00000049 [..1.1.11] #        > #
17:                    >                    [1..1.111] #        > #
18:                    >                    [.1..1111] #        > #
19:                    >                    [..1.1111] 00000a14 > 00000a14
20: 00000052:00000026 > 00000052:00000026 [...1.111] #        > #
21:                    >                    [1...1111] #        > #
22:                    >                    [.1..1111] #        > #
23:                    >                    [..1.1111] #        > #
24: 00000033:0000001b > 00000033:0000001b [...11111] #        > #
25:                    >                    [1..11111] #        > #
26:                    >                    [.1.11111] 00001165 > 00001165
27:                    >                    [..1.1111] #        > #
28: 00000064:00000062 > 00000064:00000062 [...11111] 000017df > 000017df
29:                    >                    [1...1111] #        > #
30: 00000011:0000001f > 00000011:0000001f [.1..1111] 000004a4 > 000004a4
31:                    >                    [1.1..111] #        > #
32: 0000000d:00000029 > 0000000d:00000029 [.1.1.111] #        > #
33:                    >                    [1.1.1111] #        > #
34:                    >                    [.1.11111] #        > #
35: 00000039:0000003a > 00000039:0000003a [..111111] #        > #
36:                    >                    [1.111111] #        > #
37:                    >                    [.1111111] #        > #
38:                    >                    [.1111111] #        > #
39: 0000000d:00000064 > 0000000d:00000064 [.1111111] #        > #
40: .                  > .                  [11111111] #        > #
41: #                  > #                  [11111111] #        > #
42: #                  > #                  [11111111] #        > #
43: #                  > #                  [11111111] #        > #
44: 00000044:00000000 > 00000044:00000000 [11111111] 0000131b > 0000131b
```

Figure 4.3 - Trace for Elastic 8-stage Pipelined Multiplier: The eight dots/ones between the square brackets specify if the value in the stage is a valid multiplication operation or not. Notice that when the output is not ready (denoted with a # in the far right column) the pipeline squashes bubbles in the pipeline (the dots in the square brackets disappear).