

WINDS 2010: Workshop on the Interaction between Nanophotonic Devices and Systems

Co-Located with the 43rd International Symposium on Microarchitecture
Sunday, December 5th, 2010 • Atlanta, Georgia
<http://www.csl.cornell.edu/winds2010>

Workshop Organizer

Christopher Batten
Cornell University

Technical Program Committee Chairs

David Albonese
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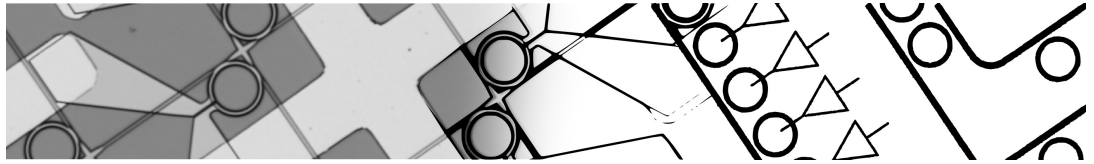
Nathan Binkert
HP Labs

Luca Carloni
Columbia University

Ajay Joshi
Boston University

Nevin Kirman
Intel Labs

Herb Schwetman
Oracle, Sun Labs



Technology scaling will soon enable high-performance processors with hundreds of cores integrated onto a single die, but the success of such systems could be limited by the corresponding chip-level interconnection networks. Nanophotonic networks are a promising direction that attempt to provide improved performance, bandwidth density, and energy efficiency compared to projected electrical networks. There has recently been significant progress at the nanophotonic device level, and there have also been many recent system-level proposals that explore how to use these devices in intra- and inter-chip networks. The goal of this workshop is to bring together device-level and system-level nanophotonic researchers to talk about their work and to share their experiences with this emerging technology.

This full-day workshop will be held on Sunday, December 5, 2010, co-located with MICRO-43 in Atlanta, GA. The workshop will include two short tutorial presentations, several invited speakers, and eight presentations selected by the technical program committee based on extended abstract submissions. Participants can register for the conference and/or the workshop on the main conference registration website.

Workshop Program (see workshop webpage for schedule and more details)

- Keynote: *The Oracle Macrochip: Architecture and Devices*, Oracle, Sun Labs
- Tutorial: *Microphotonics for Next Generation Computers*, Michael Watts (MIT)
- Tutorial: *Designing Nanophotonic Interconnection Networks*, Christopher Batten (Cornell)
- Invited Talk: *Future State-of-the-Art Electrical Interconnect*, Byungsub Kim (Intel)
- Invited Talk: *Scaling and Designing Nanomodulators for Chip-Level Integration* Sasikanth Manipatruni (GE Global Research)
- *Scalable Nanophotonic Interconnect for Cache-Coherent Multicores* R.W. Morris and A.K. Kodi (Ohio University)
- *Optically Connected Disintegrated Processor Architecture* Y. Pan, Y. Demir, N. Hardavellas, J. Kim, and G. Memik (Northwestern/KAIST)
- *Implementing System-in-Package with Nanophotonic Interconnect* M. Cianchetti, N. Sherwood-Droz, and C. Batten (Cornell)
- *System-Level Trimming Issues in On-Chip Nanophotonic Networks* C. Nitta, M. Farrens, and V. Akella (U.C. Davis)
- *EOS: A Monolithic CMOS Photonic Platform* V. Stojanović et al. (MIT)
- *Device Guidelines for WDM Interconnects Using Silicon Microrings* N. Sherwood-Droz, K. Preston, J.S. Levy, and M. Lipson (Cornell)
- *Prototyping of a 3D Integrated Intra-Chip Free-Space Optical Interconnect* B. Ciftcioglu et al. (University of Rochester)
- *Towards Chip-Scale Plasmonic Interconnects* H.M.G. Wassel et al. (UCSB/Stanford)