Cornell University

System-in-Package with Nanophotonic Interconnect

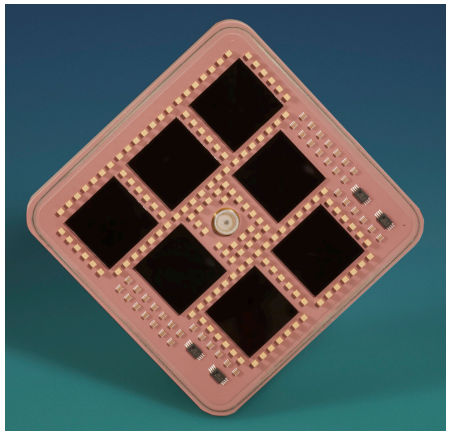
*Mark Cianchetti, Nicolás Sherwood-Droz, *Christopher Batten

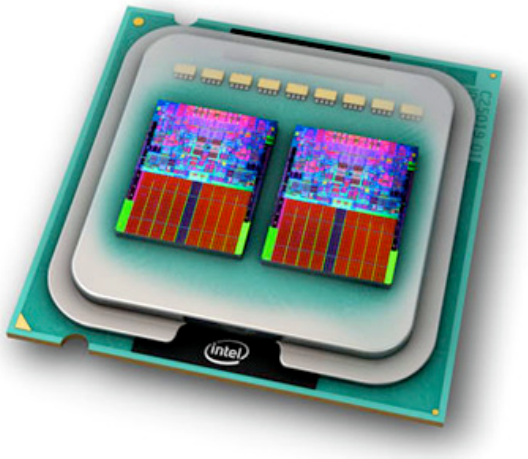
*Computer Systems Laboratory, Cornell University

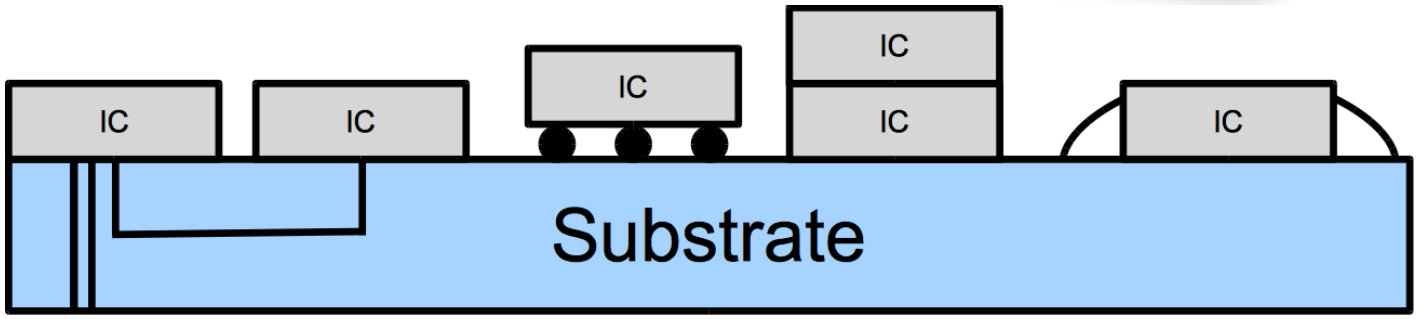
Cornell Nanophotonics Group

CSL

Electrical System-in-Package

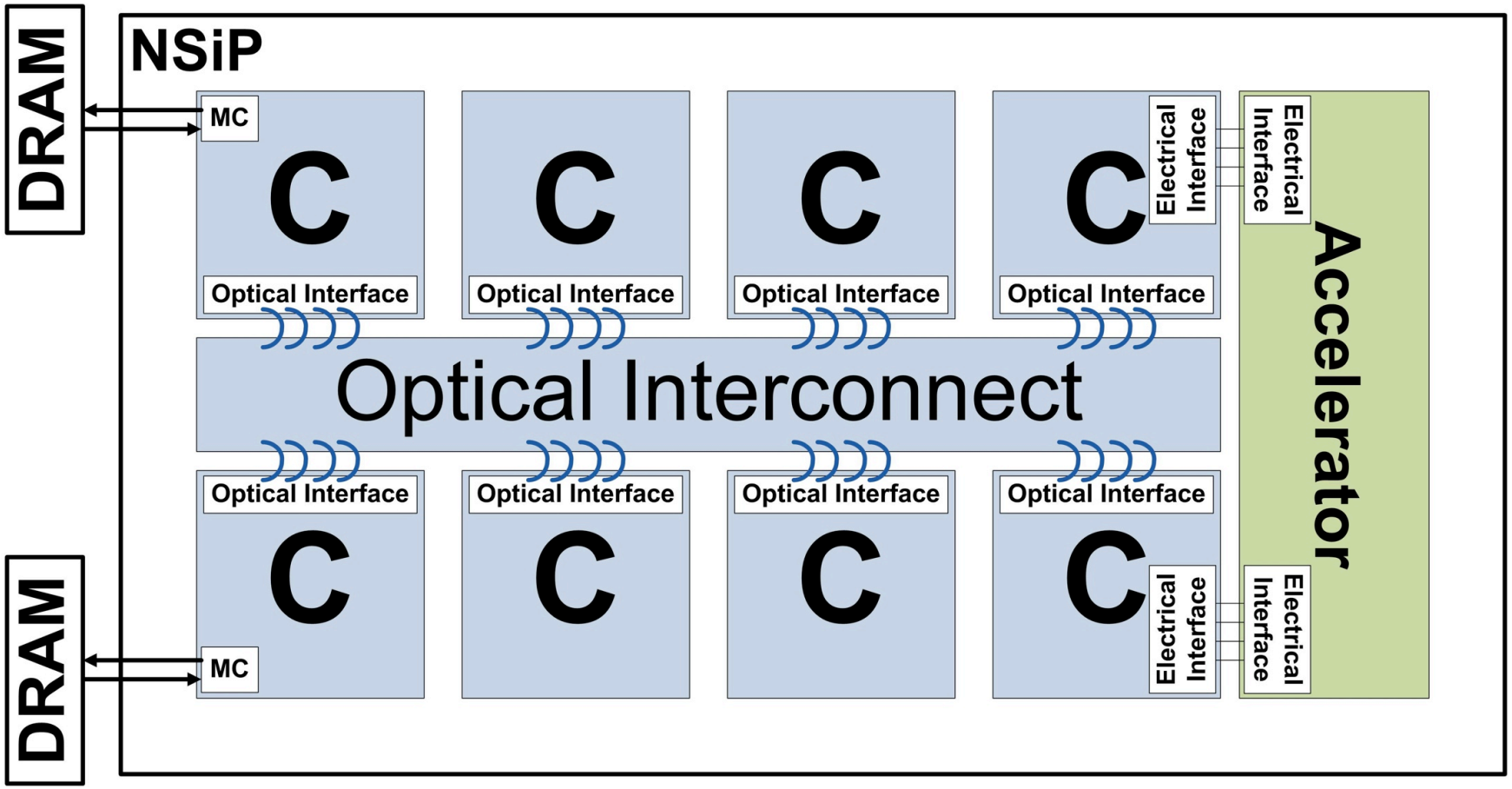






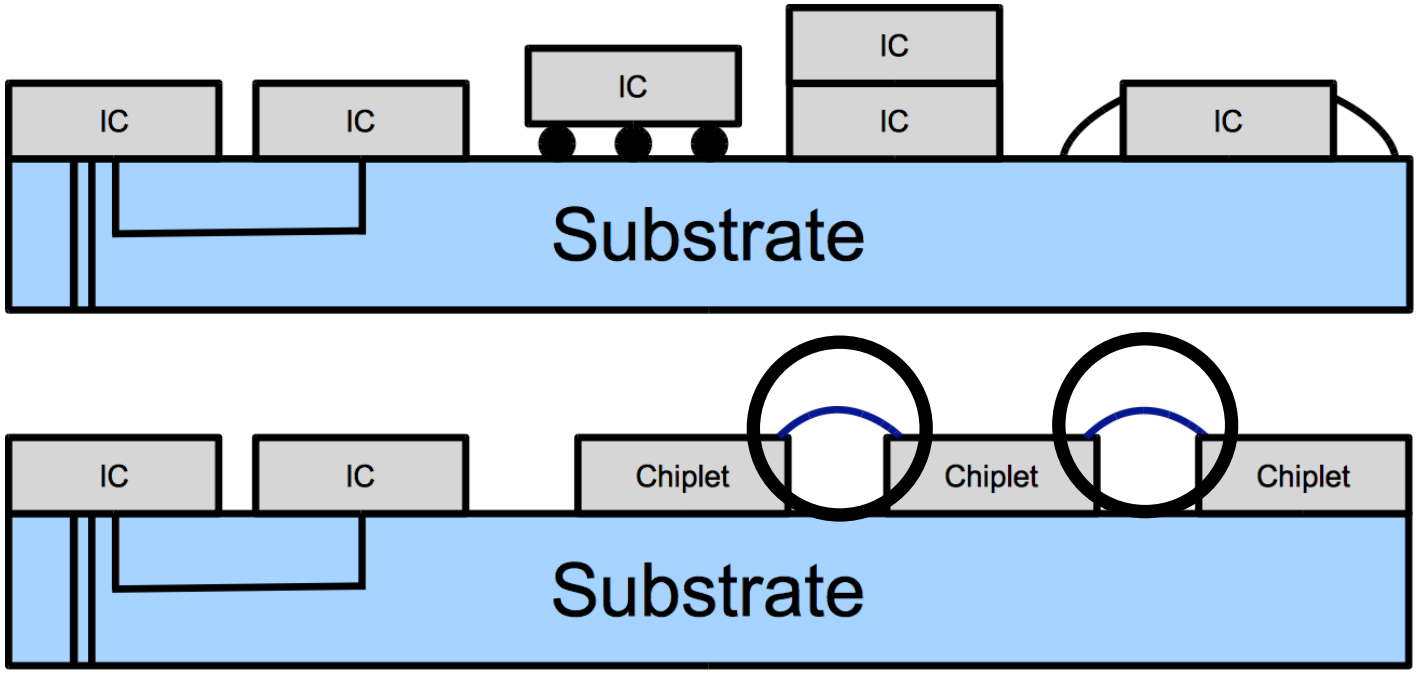
- MultiChip Module (MCM)
  - Joins multiple dies across a shared substrate
- Interconnect has lower performance and power efficiency than monolithic alternatives

Nanophotonic System-in-Package



- An NSiP contains *nanophotonic chiplets* and standard electrical chips
- Nanophotonics provides high-speed, power efficient inter-die interconnect

NSiP Versus SiP

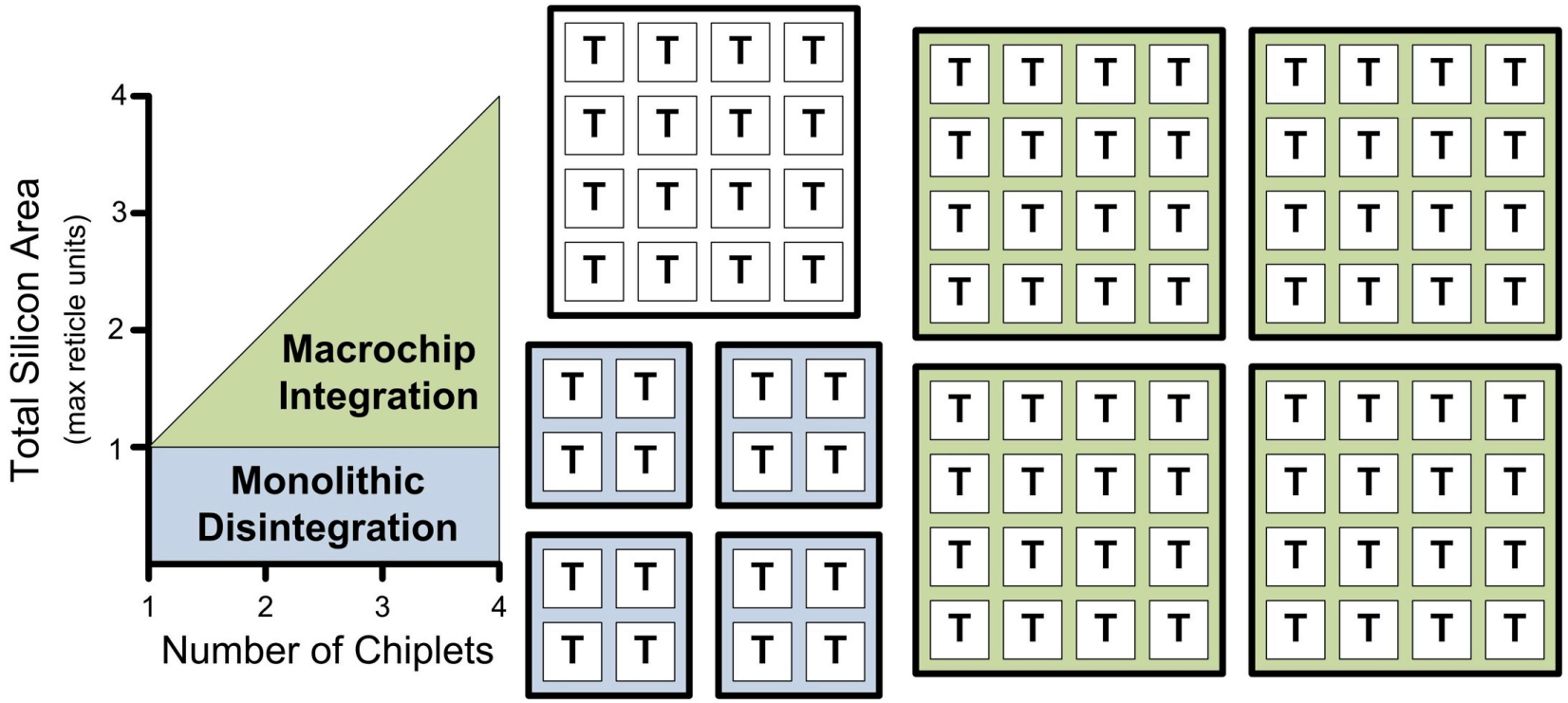


- High inter-die communication bandwidth through nanophotonics
  - Competitive with bisection bandwidth available on-chip
- Improved power efficiency over electrical communication

Talk Outline

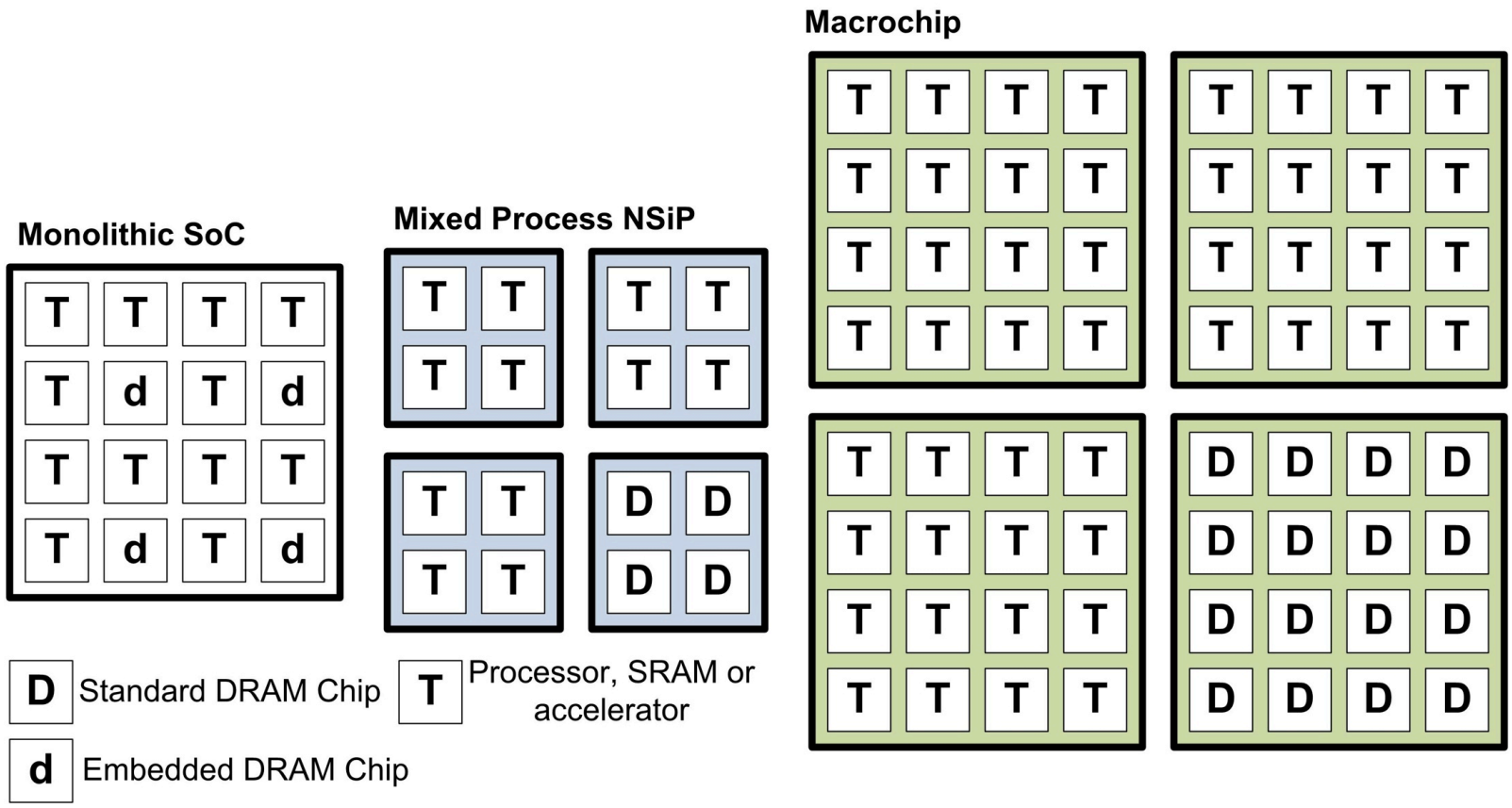
- **POTENTIAL ADVANTAGES OF NSIP**
  1. Enable systems not possible with SoC
  2. Reduce NRE via OTS chiplet composition
  3. Reduce marginal cost due to low yield
- NSiP device-level strategy
- NSiP system-level strategy
- Routing strategies and preliminary results

NSiP Integration Classes



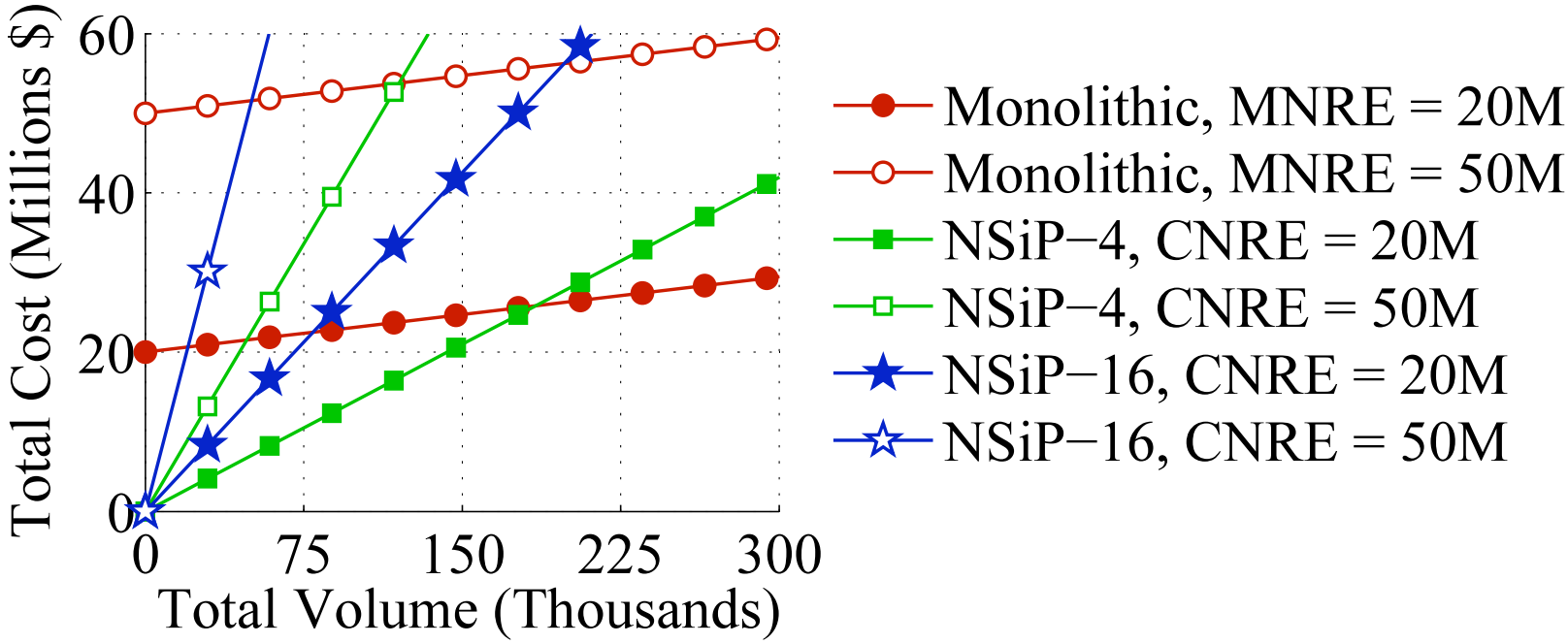
- *Monolithic disintegration*
  - Monolithic SoC divided into multiple small chips
- *Macrochip integration*
  - Permits fabrication of systems with total area beyond reticle size limitations

ADV1: NSiP Enabled Systems



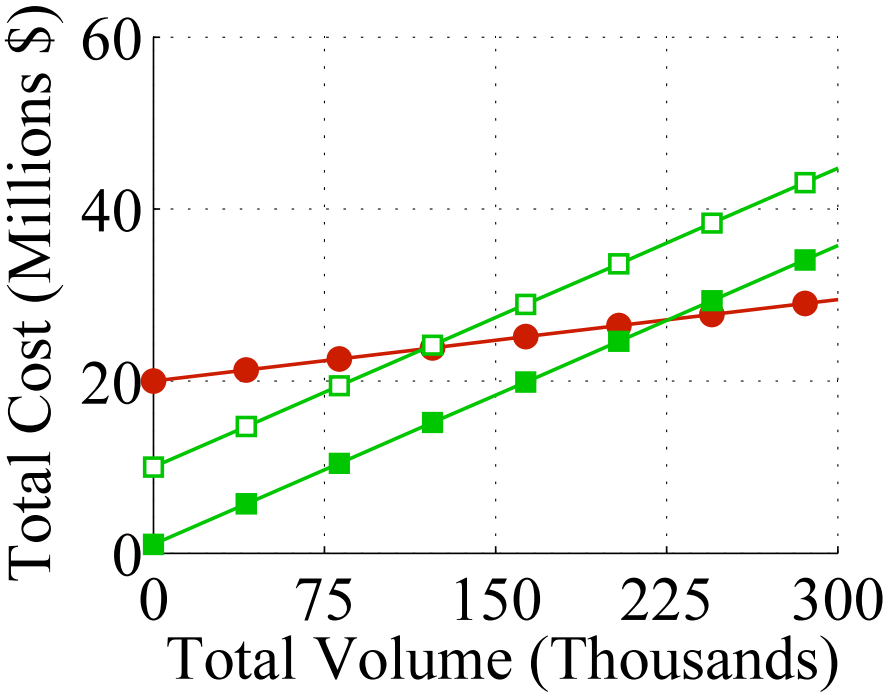
- NSiP enables systems not possible with SoC
  - Mixed process technology for increased customization
  - Macrochip integration (SoCs above reticle limit)

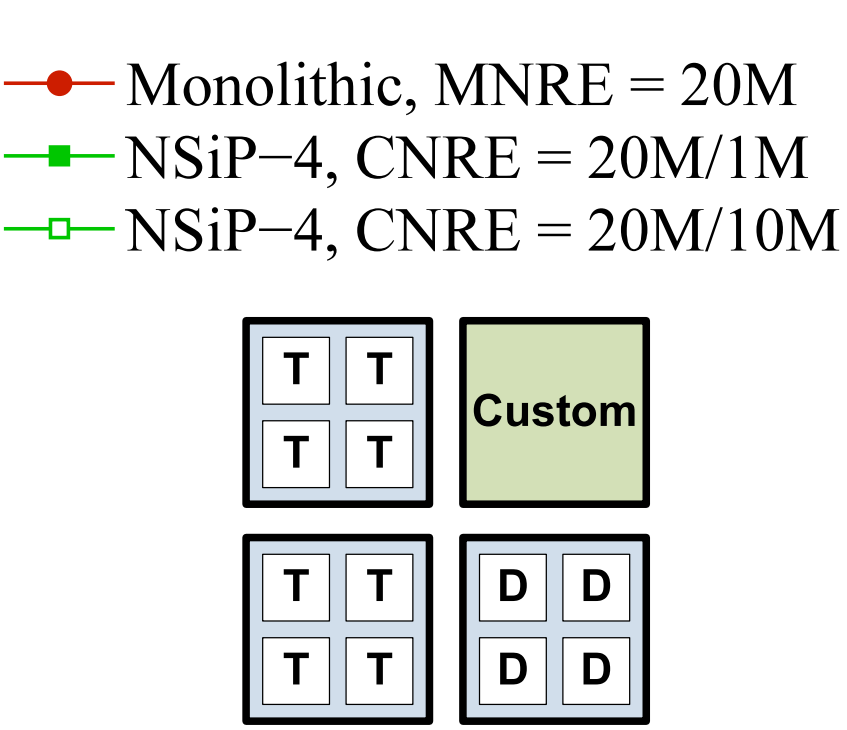
ADV2: Reduced NRE Costs



- Off-the-shelf (OTS) chiplet composition
  - Eliminates initial NRE overhead
- Economical for low to mid production volume

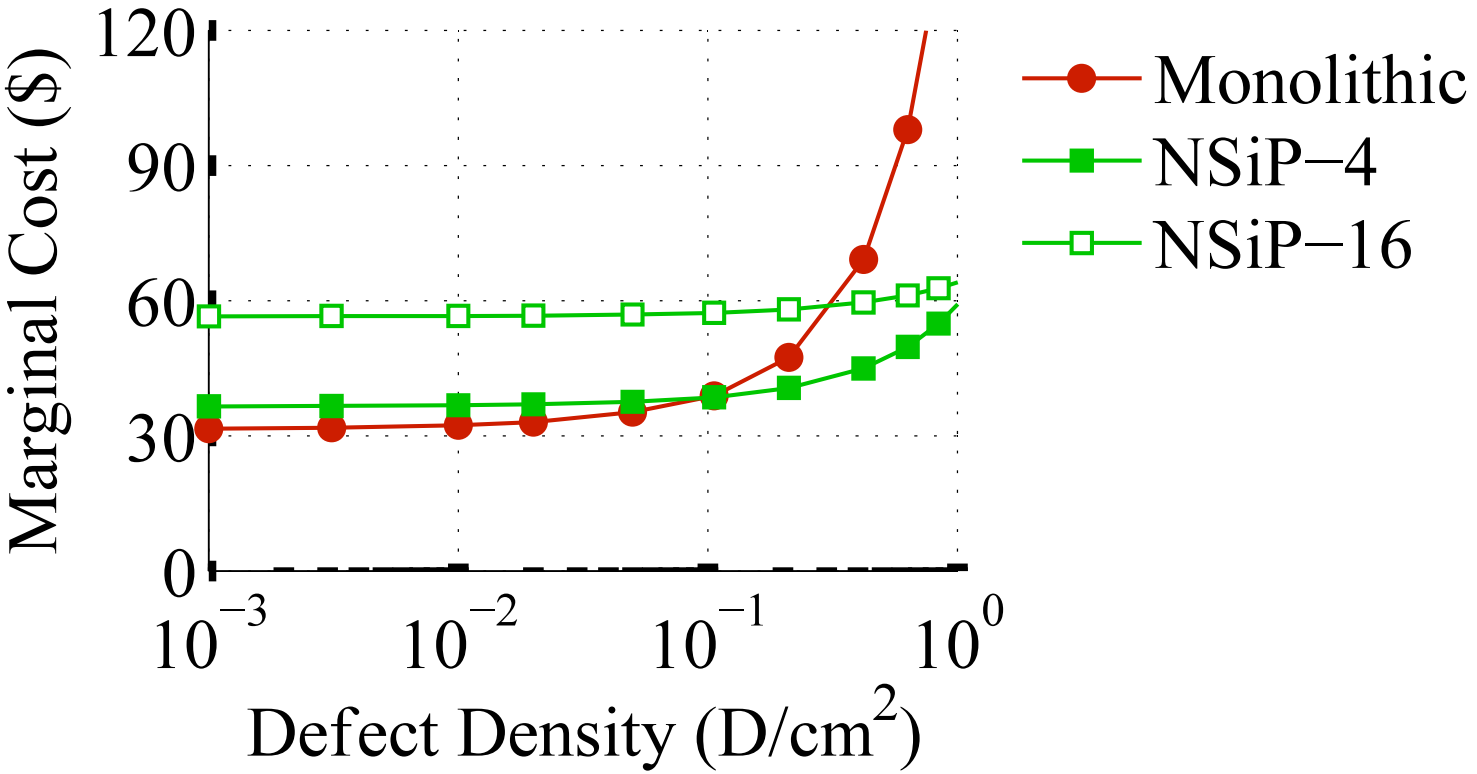
Custom Chiplet Fabrication





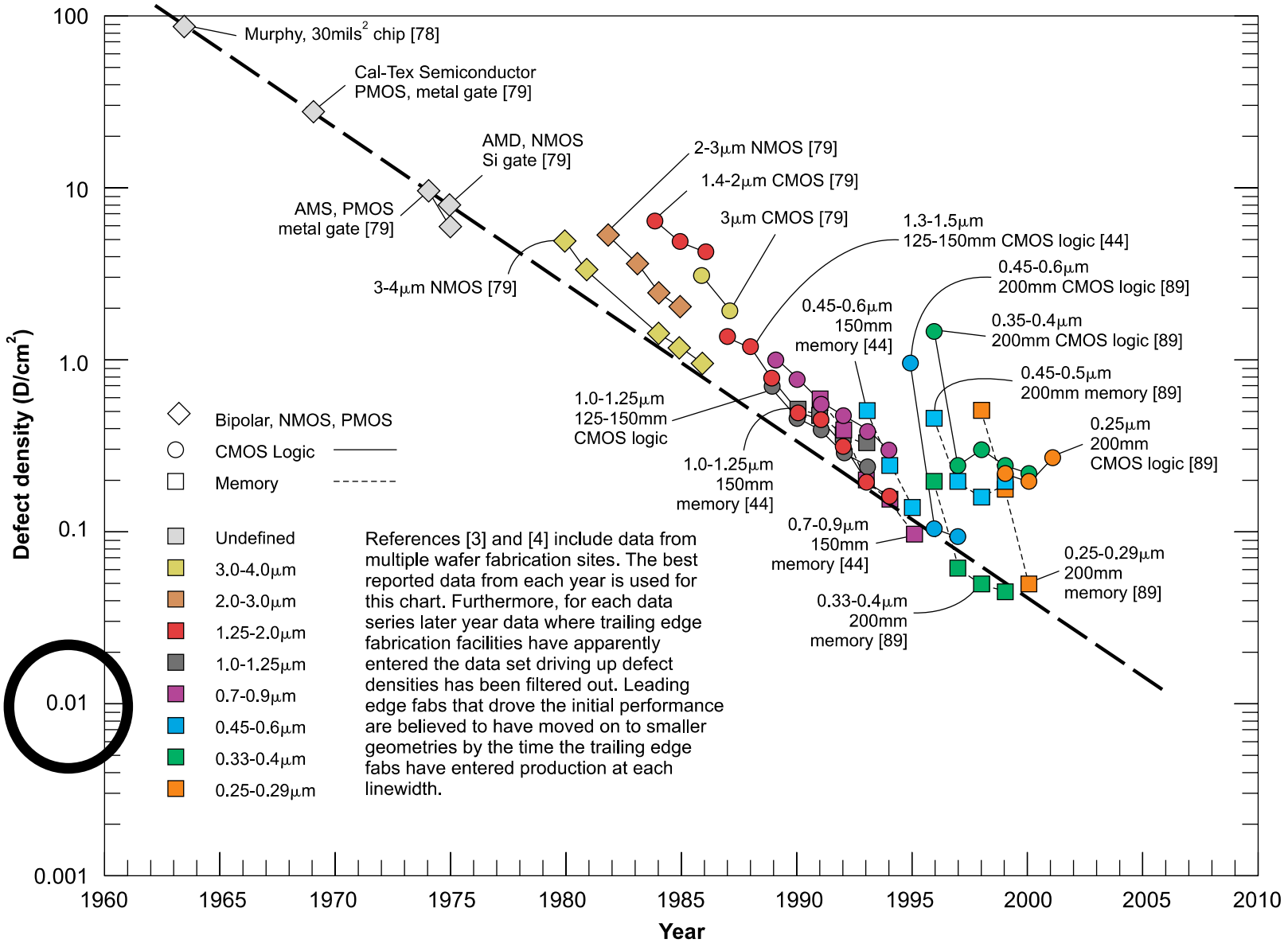
- NSiP consists of three OTS chiplets and one custom chiplet
- Custom fabricated chiplet incurs an upfront NRE overhead

ADV3: Reducing Marginal Costs



- NSiP has a lower marginal cost at high defect densities
  - May be beneficial if future processes result in significantly lower yields
- Speed binning for system yield improvement

Expected Defect Densities

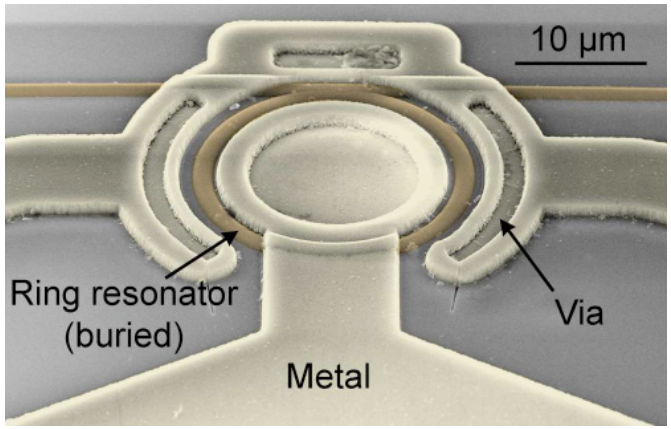


Talk Outline

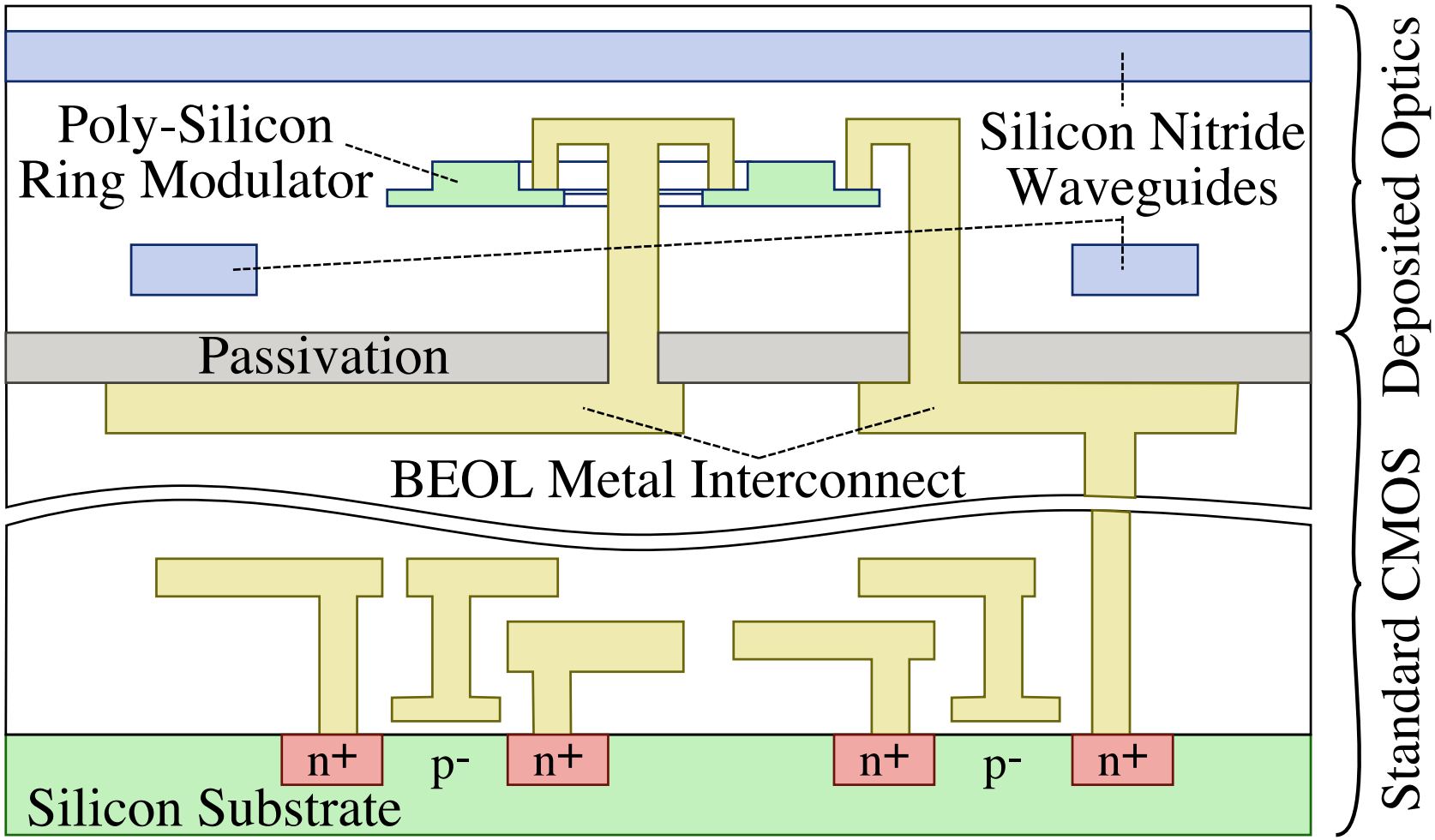
- Potential advantages of NSiP
  - Enable systems not possible with SoC
  - Reduce NRE via OTS chiplet composition
  - Reduce marginal cost due to low yield
- **NSIP DEVICE-LEVEL STRATEGY**
- NSiP system-level strategy
- Routing strategies and preliminary results

NSiP Device-Level Strategy

- Back-end-of-line (BEOL) nanophotonic technology
  - Devices can be deposited on chips fabricated in different processes
- BEOL device materials
  - Deposited poly-silicon rings
  - Multi-layer silicon-nitride waveguides
  - Germanium photodetectors
- Development of NSiP prototype
  - Chiplets fabricated in standard CMOS foundry
  - Nanophotonic devices deposited in an academic research lab



BEOL Technology



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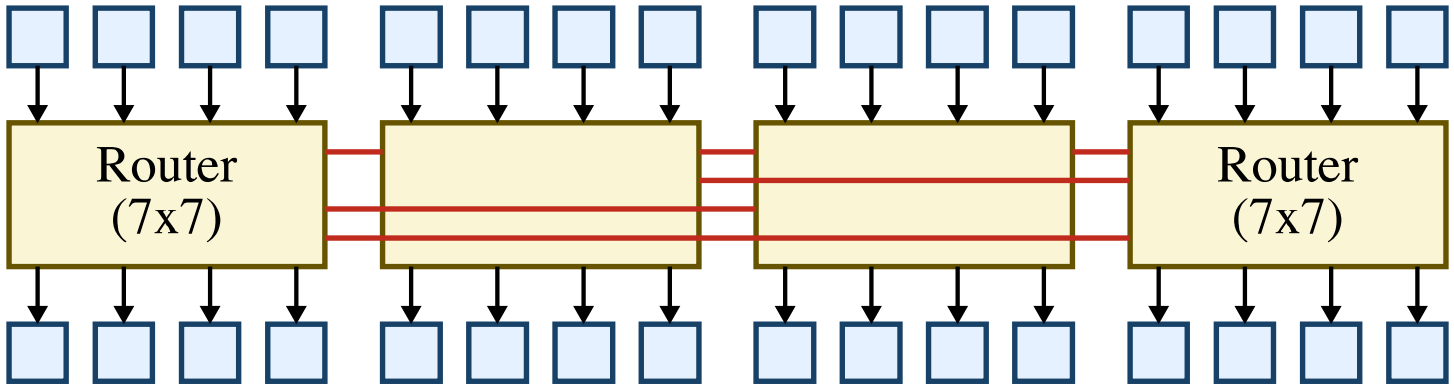
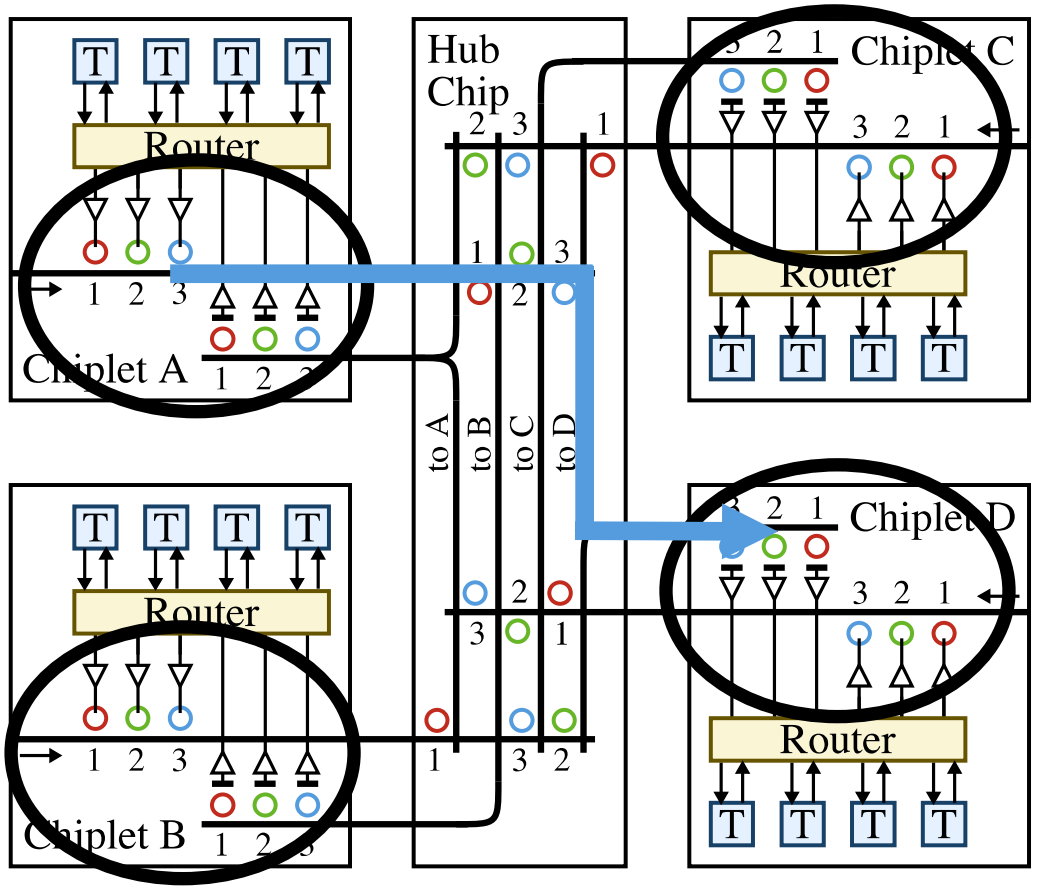
NSiP System-Level Strategy



- Chiplets are interconnected in a 2-fly flattened butterfly topology
  - Minimizes inter-chiplet communication latency
  - Minimizes optical coupling losses
- Scaling NSiP to larger number of processors
  - Increase topology radix or add second butterfly stage

NSiP Implementation



- Chiplets contain nanophotonic transmitters and receivers
- Centralized hub chip passively shuffles wavelengths between chiplets
  - Thermally isolated and optimized for nanophotonic devices

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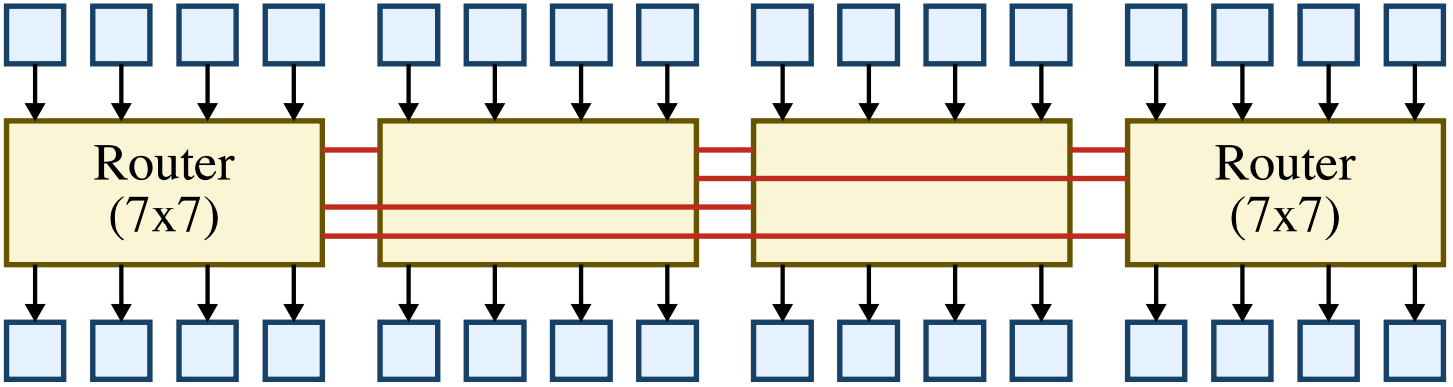
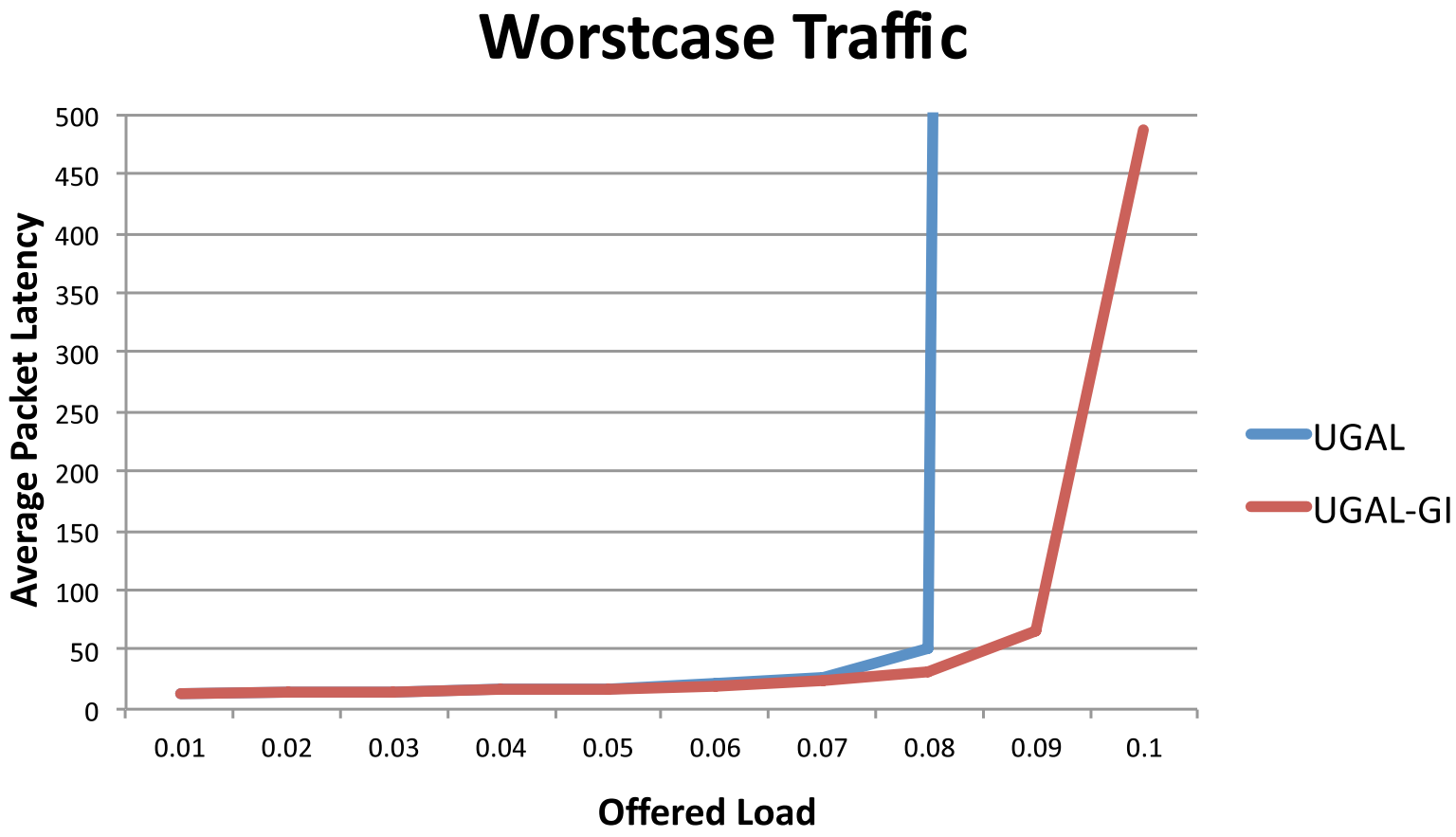
- NSiP system-level strategy
- **ROUTING STRATEGIES AND PRELIMINARY RESULTS**

Tightly Coupled Adaptive Routing

- Universal globally adaptive load-balanced routing (UGAL)
  - Minimal routing under low traffic load
  - Valiant's routing through a random node under high traffic load
- NSiP topology provides tightly coupled congestion feedback
  - Every router is connected to the others
- We propose to use UGAL with global information (UGAL-GI)
  - Adaptive decision is based on feedback from all other network routers



Example: UGAL Vs. UGAL-GI



- UGAL-GI has a 25% improvement in saturation throughput

Conclusions

- SiP has three key advantages over SoC
  - Macrochip and mixed process systems
  - OTS composition for reduced NRE
    - OTS composition with custom design
  - Speed binning for increased yield
- NSiP overcomes the performance and energy limitations of SiP
- Future Work
  - Small proof-of-concept NSiP prototype
  - Modeling larger number of chiplets